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Comparative Study of Conventional and SOI Inverters using Silvaco TCAD Tool

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Abstract: **We are living in an information age which was largely made possible by progress made in semiconductor technology and computer science. The conceptualization of integration of devices into a single chip by Jack Kilby and later its implementation by Robert Noyce in Silicon was a landmark invention in the history of humans. Later the prediction of one of the colleague of Noyce at Fairchild, Gordon Moore that components on the chip will double every 18 months and Dennard's Scaling principle paved the way for the miniaturization in electronics. 'The smaller the better' become a slogan in electronics. Miniaturization further allowed embedding intelligence into almost any gadgets of human use whether it a cell phone or an automobile or a washing machine.**

However the scaling which continued for about five decades unabated introduced new challenges to device and process engineers. Many of the challenges in the device levels were addressed by modifications in the processing techniques and introducing new materials and device architectures. Silicon on Insulator (SOI) is one such architecture which was introduced by IBM. It is expected to reduce the substrate current, lower the parasitic capacitance there by reducing the power consumption and improving the transient response of the device. In the present study comparative study of conventional MOSFET and SOI structures were carried out through simulation using Silvaco–ATLAS tool. Performance at circuit level was explored by simulating inverters made of both conventional and SOI devices. This was simulated using mixed mode feature of Silvaco TCAD. It was found that substrate current and transient response of SOI structures is much better than the conventional MOSFET. This device architecture will be of special interest for space applications were one need to employ radiation hardened devices.

1. INTRODUCTION

Since the invention of the first transistor in 1947 [1], then the integrated circuit in 1958 [2] by Jack Kilby, microelectronics progresses has been considerable, both in terms of improved performance and increased complexity of circuits that of lower production costs. Later its implementation by Robert Noyce in Silicon and the prediction of one of the colleague of Robert Noyce at Fairchild, Gordon Moore [3] that components on the chip will double every 18 months and Dennard's Scaling [4] principle paved the way for the miniaturization in electronics.

In a modern day IC there may be millions of transistors on a small piece of silicon. Naturally the fabrication and design of these IC's cannot be done without computer aids. Both the fabrication and design of these IC's require Electronic Design Automation tools (EDA). There is a need for highly precise software tools to analyze and simulate the design and fabrication of integrated circuits. Lot of research has been done and still going on these issues. As a result we have got highly useful tools for design and fabrication of IC's [5].

MOSFET transistors on silicon used in CMOS architecture are the main craftsmen's of this continual progression and overwhelmingly dominate semiconductors market. The improved performance of these transistors always requires more imagination on the part of component designers in order to respect the new requirements of electronics industry for faster, smaller, low power and reliable ICs. However, with this frenetic race towards miniaturization, device feature sizes progress into deep-sub-micrometer regime under 50nm node for realizing better device performance and higher integration densities.

Accordingly, MOSFETs characteristics degrade, and some effects known as short channel effects appear, worsening the correct operation of CMOS devices [6]. The importance of these effects and the complexity of the methods used to counter them led to the development of alternat1ive transistor structures (new architectures) and new materials. These new architectures can be the possible alternatives to the bulk traditional MOSFETs. Thus, to achieve this goal laid down by the "International Technology Roadmap of Semiconductor" [7], new architectures using SOI MOSFETs had been very seriously considered to replace bulk MOSFET architecture. Thus, SOI technology is considered to take the CMOS processing to its ultimate scalability in order to highlight the qualities.

2. SOI TECHNOLOGY

The market has been growing and making tough demands for semiconductor integrated circuits, to consume less power, have higher integration, have multi-function capability, and be

faster. In electronics, an SOI MOSFET semiconductor device is a Silicon on Insulator (SOI) MOSFET structure in which a semiconductor layer e.g., silicon , germanium or the like, is formed above an Insulator layer which may be a buried oxide (BOX) layer formed in a semiconductor substrate. The use of a layered SOI substrate in place of conventional silicon substrate in the semiconductor manufacturing. It differs from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire. In SOI technology small islands of silicon are formed on an insulator film. Using SOI fabrication process coupled with lateral isolation techniques we can get circuits with very small parasitic capacitances and latch up free circuits. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects. One of these parasitic is the capacitance between diffused source and drain and substrate. This capacitance increases with substrate doping and becomes larger in modern submicron devices where doping concentration in the substrate is higher than in previous MOS technologies .In addition latch up effect can be reduced by using SOI-MOSFET [8].

Conventional semiconductor devices are highly prone to ionizing radiations and cosmic rays. Such radiations can cause electron-hole pair generation in the Silicon substrate and thereby causing a large leakage current. This not only causes the increase in static power dissipation but also can change the data stored in semiconductor memories popularly known as single-event upset. Radiation- hardening i.e. prevention of radiation-induced effects is of paramount importance in space applications where the systems are exposed to cosmic radiations [9]. The presence of BOX layer in SOI prevents devices and circuits from this radiation effects. So, SOI is considered as the best candidate in space applications rather than the conventional one.

3. SOI-MOSFET

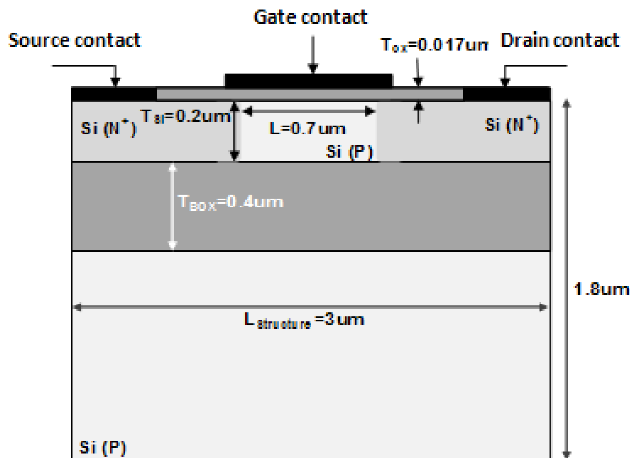

Figure 4: Basic structure of SOI n-MOSFET.

The SOI-MOSFET device contains the traditional three terminals (source, drain and gate which control a channel in which current flows from source to drain). Figure 1 shows the basic structure of a SOI-MOSFET with drain, source and drain terminals.

The dimensions of the structure shown in figure 1 are followed for modeling of the structure in the Table 1.

Table 1: Parameters of SOI n-MOSFET transistor.

Parameter	Value
Drain length and Source length	1um
Gate length	1um
Channel length	0.7um
Gate oxide thickness T_{OX}	0.017um
Silicon film thickness T_{si}	0.2um
Buried oxide thickness T_{BOX}	0.4um
substrate Thickness	1.2um
Depth junction	0.52um
Substrate concentration	$1x10^{17}$ cm^{-3}
Drain and Source concentration	$1x10^{20}$ cm^{-3}

The physics of the SOI MOSFET is highly depended on the thickness and doping concentration of the silicon film in which they are made. Two types of devices can be distinguished: devices in which the silicon film in the channel region is never completely depleted called partially-depleted SOI or PDSOI. The other type of device where silicon film can be completely depleted is called fully-depleted SOI or FDSOI.

In PDSOI the silicon film thickness is larger than twice the value of maximum depletion width. In such a case there is no interaction between the depletion zones arising out from the front and back interfaces. A neutral region exists beneath the depletion regions. If this neutral peace of silicon called body is connected to ground by a body contact the characteristic of the device will be exactly those of a bulk device.

In a FDSOI the silicon film thickness is smaller than maximum depletion width. In this case the silicon film is completely depleted at threshold, irrespective of the bias applied at the back gate [10].
In this present study, PDSOI on silicon is studied.

4. EXPERIMENTAL MATERIALS & METHODS

4.1 Device Simulation

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena, which determine

electrical characteristics of semiconductor devices. We know the real-time fabrication methods for SOI-MOSFET device. First of all the silicon substrate of SOI-MOSFET device was modeled by followed by thick oxide layer which is an insulator with again with another silicon layer are made using Atlas-simulator (SILVACO). The thick silicon dioxide layer is also known as the Buried Oxide layer (BOX). The silicon layer above the BOX is where the device is fabricated, and the silicon underneath the BOX, can handle the wafer during fabrication process, and does not affect device performance to any great degree. All the three terminals i.e. gate, drain and source are shown below:

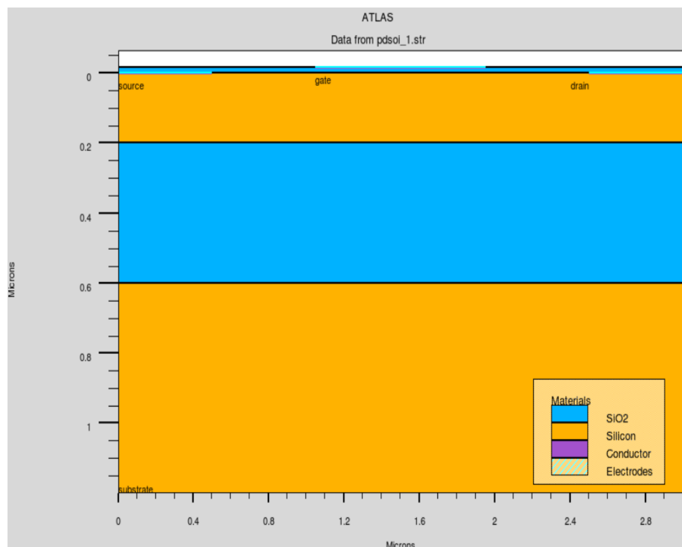

Figure 5: SOI-MOSFET structure in Atlas simulator.

The conventional MOSFET can also be simulated like this except the buried layer. Figure 3 shows the conventional-MOSFET structure:

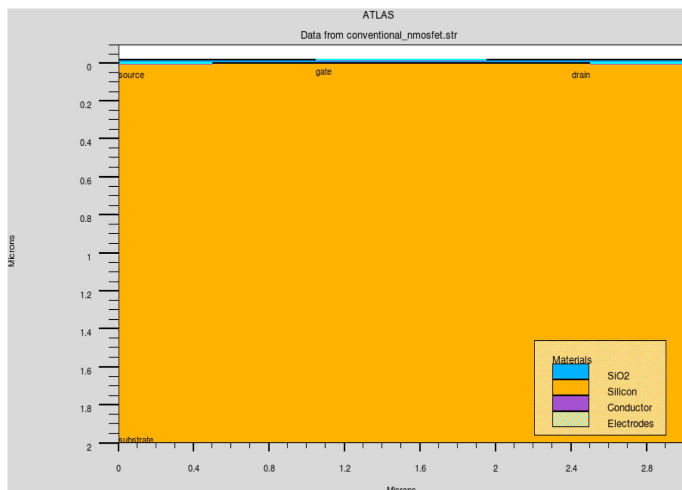

Figure 6: Conventional-MOSFET structure in Atlas.

4.2 Circuit Simulation

Mixed Mode simulation allows compact model devices to be replaced by physically-based device models. This is a special feature of Atlas simulators.

In order to do the circuit simulation of our device structures as an inverter, we make use of one library model device (MN) of the n-MOSFET and other is prepared-ATLAS device - the ATLAS n-MOSFET (AN) as enlightened in below figure 4. Input voltage, VIN is applied to the node 1 in the circuit and then at node 2, output of first transistor AN is generated. This output acts as the input for the second transistor, which in turn give an output at node 3. It has been clarified from figure that such type of circuit acts as like an inverter pair. In this circuit, voltages at first and third nodes; V {1} & V {3} respectively are same and voltage at second node, V {2} is complementary to both of these.

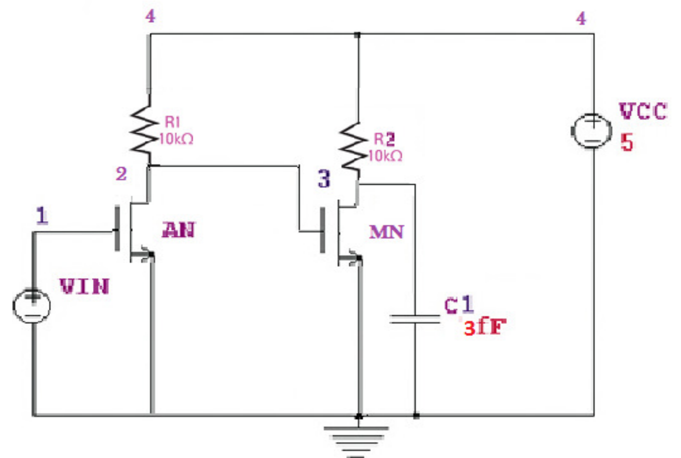

Figure 7: NMOS inverter with transistors AN (ATLAS), MN (compact model) devices.

The two types of analyses are performed to the circuit shown in figure 4:
(1) DC analysis
(2) Transient analysis

5. SIMULATED RESULTS WITH DISCUSSIONS

For computer simulations of the Silicon-on-Insulator device, Deckbuild provides the interface for changing and altering the input code to the device simulator. Atlas allowed us to create a simplified version of the SOI device in which it was easy to vary parameters such as gate length and doping.etc .The first step is to model the structure with proper dimensions then voltage will be applied to the gate for determination of I-V curves.

For this we need to write the code for obtaining I-V curves I_d-V_{gs} (Figure 5) as shown below:

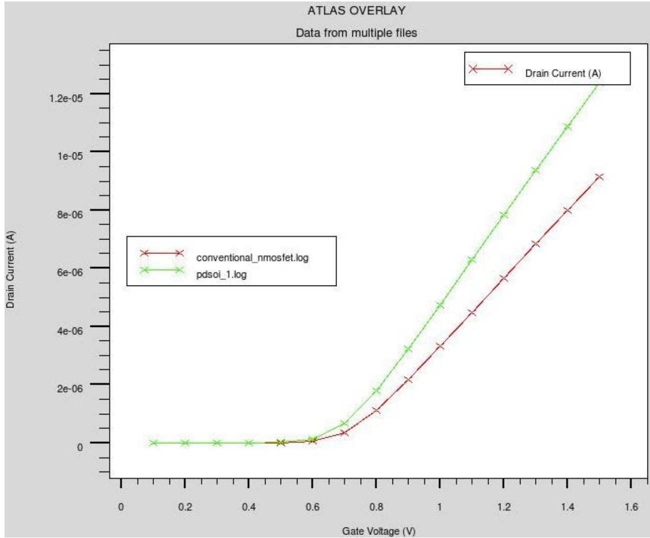

Figure 5: V_T overlay of Conventional & SOI-MOSFET.

Table 2: Threshold Voltages

Sr. No.	Device Structure	Threshold Voltage, V_T(V)
1.	Conventional n-MOSFET	0.667546
2.	SOI-n-MOSFET	0.642499

Comparisons between circuit simulations of conventional & SOI-MOSFET as an inverter circuits:

1) DC analysis of both device circuits is shown in figures 6, 7.
2) Comparison of transient analysis of both device circuits are shown in figures 8, 9, & 10.
3) Also in figure 11, comparison of substrate currents are discussed.

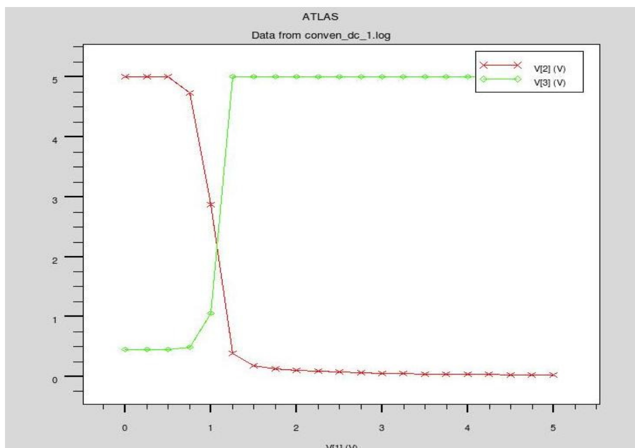

Figure 6: DC Analysis of a conventional n-MOSFET.

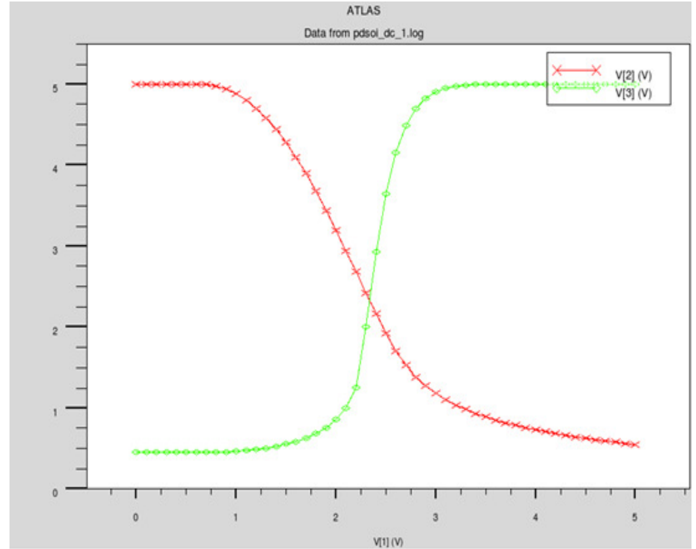

Figure 7: DC Analysis of a SOI-n-MOSFET.

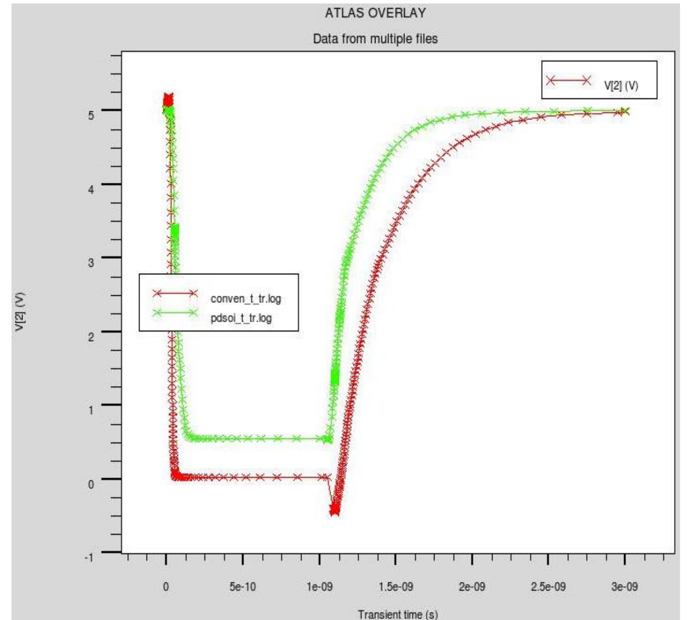

Figure 8: Comparison of transient analysis of two transistors at node 2 in the inverter circuit.

From the above figure 8, we see that transient response of a SOI-based n-MOSFET as an inverter circuit is better, i.e. in other words its switching speed is fast than the conventional n-MOSFET. Hence we can conclude that the SOI-based n-MOSFET is more advantageous in terms of performance than the conventional n-MOSFET.

For better performance, we know that substrate current must be small and from above figure 11, we see that substrate current of a PDSOI structure is smaller than the conventional transistor structure.

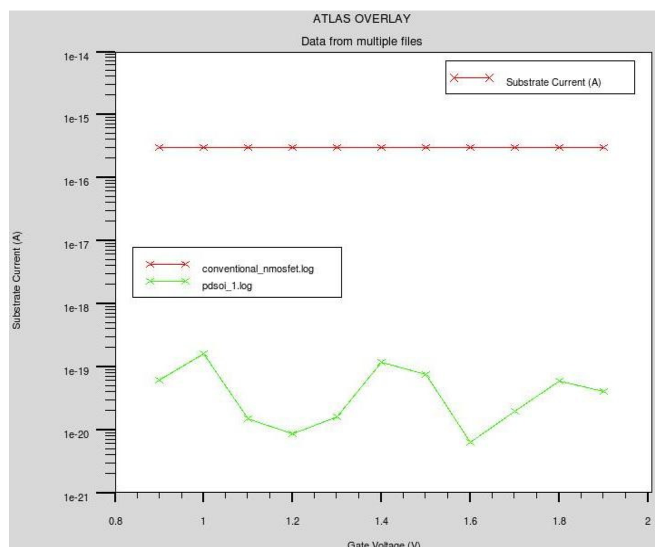

Figure 8: Comparison of substrate currents of the structures – PDSOI & Conventional n-MOSFET.

In this case, we apply a constant drain voltage of about 0.1 V and we ramp the gate voltage from 0.8 V to 2V. Consequently, we extracted the substrate current of the various structures when $V_{GS} > V_T$. This is shown in the figure 8 where the substrate currents of both two structures FDSOI and PDSOI are nearly in the range of $1e^{-19}$ to $1e^{-21}$ Amperes. These are smaller in comparison to conventional n-MOSFET structures which has a range of $1e^{-15}$ to $1e^{-16}$ Amperes.

6. CONCLUSION

There is a marked increase in the switching speed of the SOI structure .This is mainly attributed to the reduction in substrate capacitance due to the incorporation SiO_2 buried layer. Another major advantage of SOI as observed through simulation is that there is 3-4 orders reduction in substrate current in SOI structures as compared to conventional structures. Both these results are encouraging for employing these devices in space applications.

However there are limits to what the simulation software can do. Since these programs are computer simulations, and not physical devices, some device variation due to fabrication methods and certain unexpected physical interactions on these devices have the possibility of not being properly simulated. These programs do simulate responses based on the physics of different elements present in the created devices, and they are limited to physical processes considered in the model. These simulations should be used as a guideline when researching new technology, not as a complete replacement for the fabrication and characterization of physical prototype devices.

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