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Simulation of Radiation Hardened SOI Structure for mitigation of Single Event Upset

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Abstract: **Single Event Upset (SEU) is a change of state caused by a high-energy particle strike to a micro-electronic device. These type of errors in electronics industries use to describe a phenomenon which causes electronic devices to lock up or unstable state. This natural phenomenon happens to every digital electronic device. This paper describes the 3D view interaction of charged particles with semiconductor. To showing single event upset (SEU) effects phenomenon 3D-MOSFET is designed at 90 nm technology. Variation of drain current, shifting of threshold voltage due to fall of particle beam has been simulated. To mitigate these errors SOI architecture were used and after simulation result shows that SOI technology is right candidate for minimising SEU effects.**

1. INTRODUCTION

A state change (*flip*) of a single data bit storage or memory cell caused by an SEU. An SEU can affect the configuration memory cell states, the block RAM contents, a CLB DFF, a LUTRAM, or SRL16 memory cell [1]. These types of errors are called soft errors because such kind of errors do not permanently damaging to the transistor's or circuit's functionality unlike the case of single event latch-up (SEL). These upsets are random in nature, do not normally cause damage to the device, such as memory. The result of upsets in devices is the data corruption. When charged particles strike the silicon substrate of MOS devices, they leave an ionization trail. Similarly, when a high-energy particle such as a neutron strikes the substrate, it collides with atoms in the substrate, leaving a shower of charged particles which then form an ionization trail. If the resulting deposited charges from these particles are sufficient, then it can change the state of a data bit, memory bit or flip flop. Specifically, the electron-hole pairs generated by the interaction of an energetic charged particle with the semiconductor atoms changes the stored information in the memory cell.

Radiation both particle and electromagnetic wave is generally classified as being either ionizing or non-ionizing. The basic difference between the two is energy. Ionizing radiation has sufficient energy to emit electrons from atoms, thus creating ions. Examples of ionizing radiation are alpha and beta particles, protons, X-rays, and gamma rays [2]. Neutrons are not directly ionizing, but the resulting radiation from their collisions with nuclei is ionizing. These particles can come directly from radioactive impurities and cosmic rays or indirectly as a result of high-energy particle interaction with the semiconductors. Galactic cosmic rays (GCR) comprised of high-energy particles, overwhelmingly protons, impacts the major effects on the semiconductor devices [2-3]. Silicon on insulator (SOI) and silicon on sapphire (SOS) are often used to further reduce or eliminate susceptibility [5].

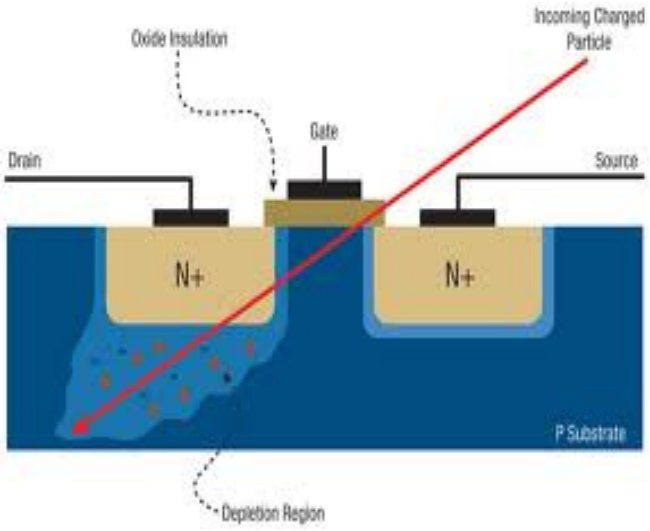

Fig.1. Particle Beam Effects in N channel MOSFET [6]

2. SEU PHENOMENOLOGY

Single event upset in semiconductor devices, charge collection is originated by the rate at which electrons and holes recombine after they are generated in or close to the depletion region. Because the speed of charge carriers is essentially directly proportional to the electric field strength, a reduction in the electric field induces a proportional increase in the rate of charge recombination, hence reduced residual charge. The thickness of the depletion region is approximately proportional to the square root of the applied field strength. Therefore, the volume in which the charge collection is effectively carried out is decreased by the square root of any reduction in the field strength [3-4]. To cause upset, the collected charge must overcome the charge stored at the sensitive node. Because the stored charge is proportional to the bias voltage, reducing the bias causes a proportional decrease in the critical charge.

Analytically then, one would expect the effect of reducing the bias voltage on the sensitive volume size to be small as compared to the effect on the electron-hole recombination rate. In opposition to these effects is the decrease in stored charge at the sensitive node. The SEU test results reported seem to indicate that the decreased critical charge predominates, hence the increased SEU susceptibility observed in the tests [4].

3. DESIGN AND MATERIALS

To demonstrate a SEU effect 3D MOSFET as well as SOI FINFET is designed. First we make a geometry of N channel 3D MOSFET using Silvaco^{TM} DEVEDIT 3D Tool in which we define various regions which are Substrate, Gate Contact (G), Drain (D) and Source (S) and then doping is done to drain, substrate and source regions. Material of various regions are defined which are shown in Table 1 below. The material used gate contact is poly silicon (N-polySi), drain, source and substrate contact is aluminium (Al) and rectangular gate region lies on top of the bulk separated by a thin silicon oxide dielectric.

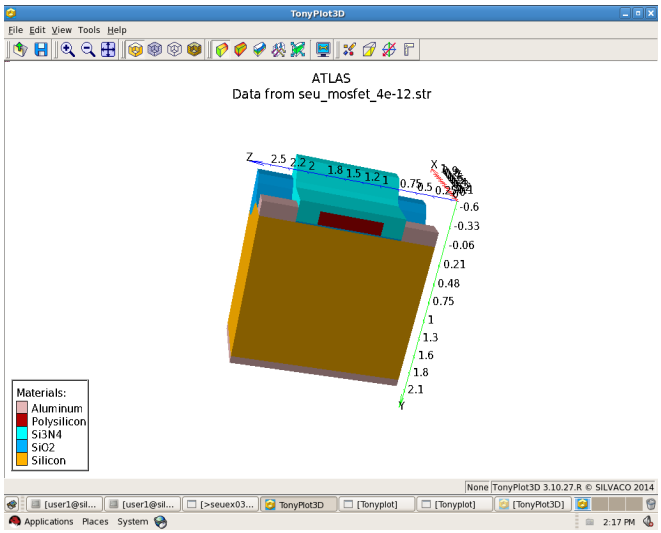

Figure 2. Device structure of 90nm 3D-NMOS

Table 1. Regions and Material used in N Channel MOSFET.

Region	Material
Substrate	Silicon
Substrate Contact	Aluminium
Spacer	Nitride
Drain	Aluminium
Source	Aluminium
Gate	NpolySi
Oxide	Sio_2

Then by the use of atlas simulator we generate the particle beam having particle density $1e^{+18}$ and radius 0.05µm [8]. Table 1 shows regions and materials used in simulation of device. Table 2 shows doping and profiles used in device. Table 3 shows the particle density and radius of the beam.

Table 2. Doping Profile.

Name	Type	DOPING
Body	Acceptor	1e+17
Drain	Donor	1e+20
Source	Donor	1e+20

Table 3. Beam radius and Particle density

Particle density	1e+20
Beam radius	0.05µm

4. RESULTS AND DISCUSSION

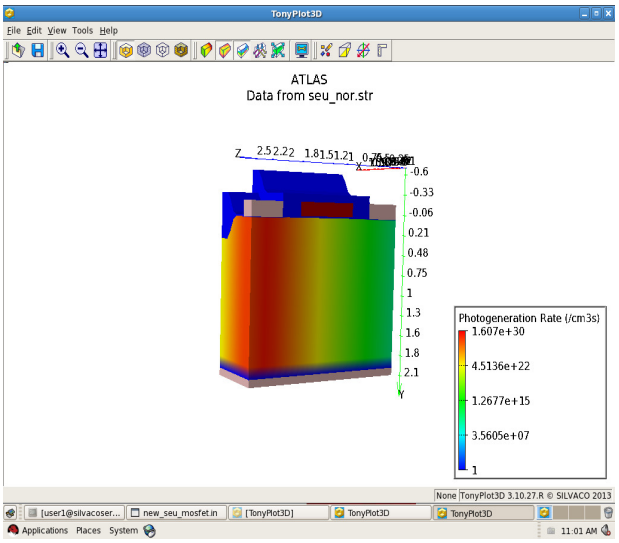

Figure 3. Photo-generation rate at normal Incidence in 3D MOSFET

Fig. 2 shows the device structure of 90nm 3D MOSFET. To show the effect of SEU charged beam of particles is incident on drain terminal. To showing the effect of SEU in bulk of the device incident beam is fall at two different angles, one normal to the plane of drain terminal and other one is oblique to drain terminal. Fig. 3 and Fig. 4 show the photo-generation effects at normal incidence and at oblique incidence of particle beam at the drain terminal of 3D MOSFET. It is observed from the figure that photo generation effect is more (larger volume of bulk) in oblique incident as compared to normal incidence, hence it is concluded that e^- hole pair generation

and recombination is increases as depth of penetration of beam increases in the substrate of the device. Fig. 5 and Fig. 6 shows the electron concentration in 3D MOSFET at normal and oblique incidence of particle beam. For showing the electron concentration effect the MOSFET is switched to ON condition by applying suitable voltage biasing and simultaneously incident the beam at the drain terminal.

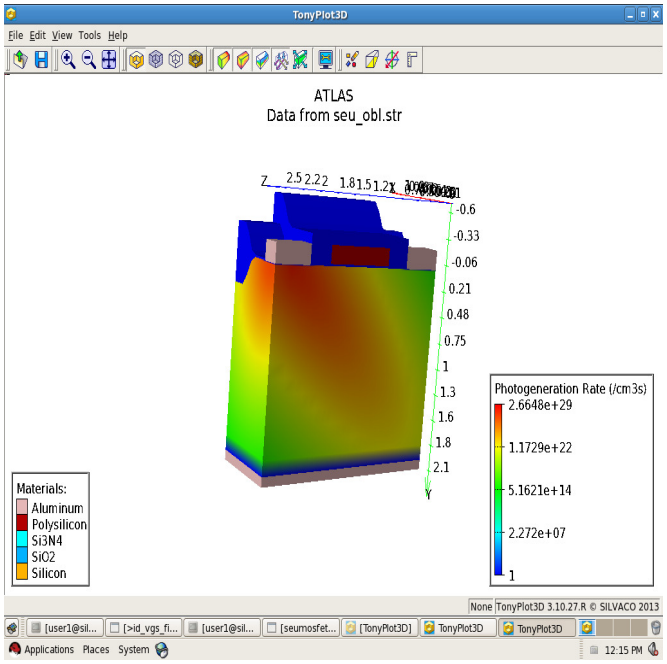

Figure 4. Photo-generation rate at oblique incidence in 3D MOSFET

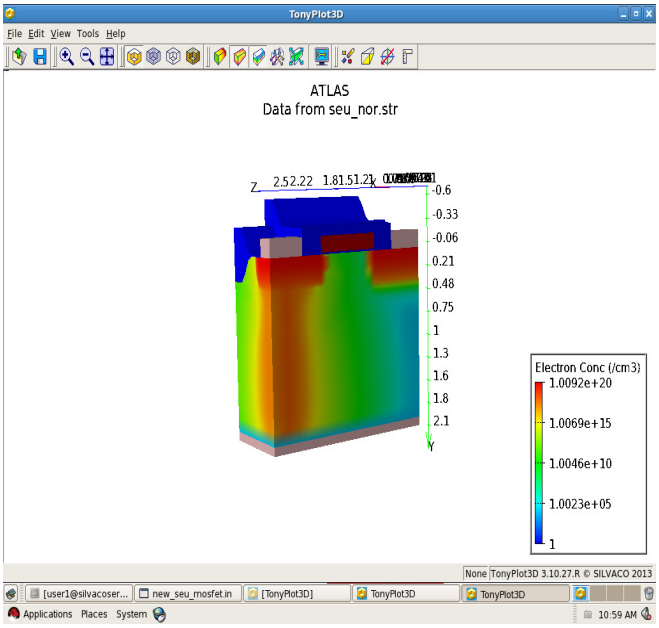

Figure 5. Electron concentration at normal incidence in 3D MOSFET

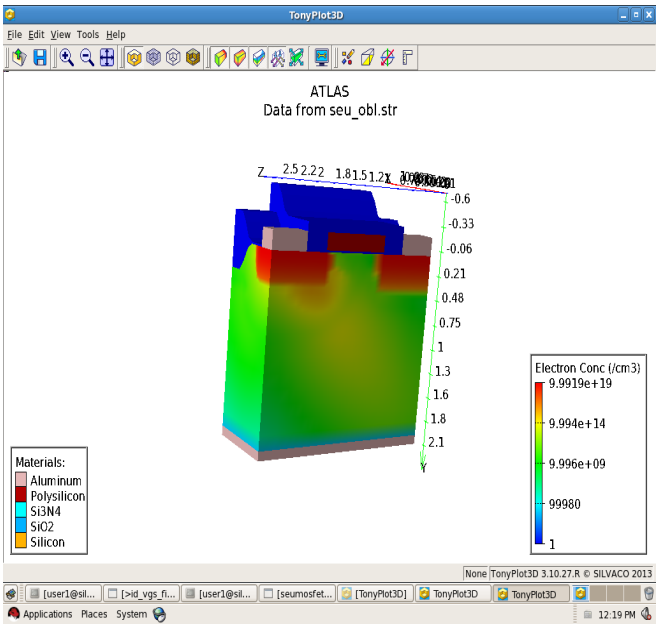

Figure 6. Electron concentration at oblique incidence in 3D MOSFET

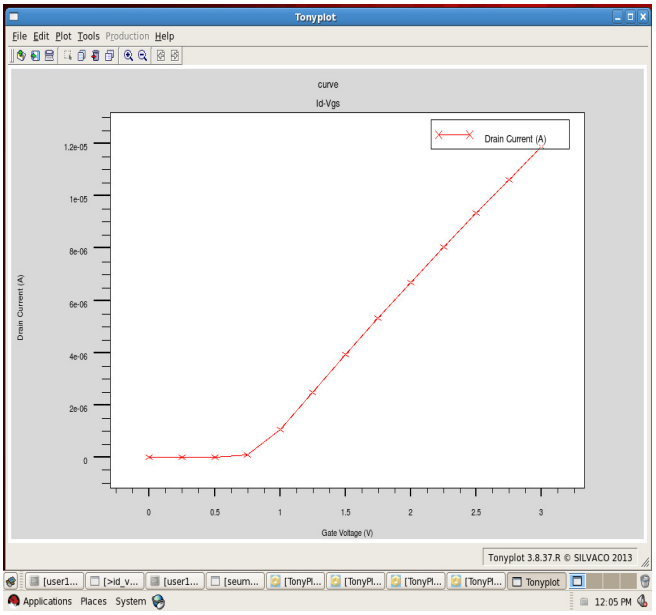

Figure 7. Drain current Vs Gate voltage curve in 3D MOSFET

Fig. 7 shows the Drain current versus Gate voltage characteristics. By this curve, the value of threshold voltage (V_{TH}) can be found out. The minimum voltage at which channel starts creating is called threshold voltage. When $V_G < V_{TH}$, the current $I_D \sim 0$ but the current start increasing when $V_{TH} \geq V_T$. The transient simulation is performed for showing the effects of SEU generation. Fig. 8 shows the transient simulation of the device at normal as well as oblique incidence. Transient simulation is perform by applying the

transient pulse ranging 1 ps to 0.1 µs, To analyze the effect of carrier generation in device, the transient characteristics of drain terminals are measured. Simulation result shows that peak of generation (t=4 ps). The simulation results shows the change in drain current in normal incidence as well as in oblique incidence. The peak of the current for the oblique incidence is observed to be slightly higher than for the normal incidence.

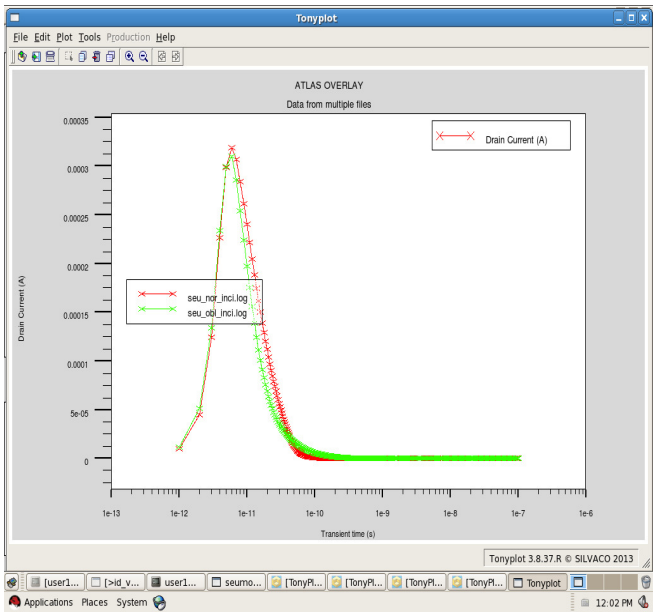

Figure 8. Transient simulation of normal and oblique incidence in 3D MOSFET

4.1 Mitigation of SEU by SOI Architecture

Previous result shows that particle radiation has significant effect in bulk devices. For showing SEU effect can be minimised by using SOI devices. To demonstrate this SOI FINFET was designed using SILVACO™ DEVEDIT 3D tool. The geometry, material regions, doping profiles, electrodes of the SOI FINFET is defined. Table 4 shows regions and materials used in simulation of device. Table 5 shows doping and profiles. After finalizing the structure its device simulation is performed using ATLAS device simulator. Fig. 9 shows the SOI FINFET device.

Table 4. Regions and Materials for SOI FINFET.

Region	Material
Channel	Silicon
Drain	Aluminium
Source	Aluminium
Gate	N poly
Oxide	Sio_2

Table 5. Doping Profile for SOI FINFET

Name	Type	DOPING
Body	Acceptor	1e+18
Drain	Donor	1e+21
Source	Donor	1e+21

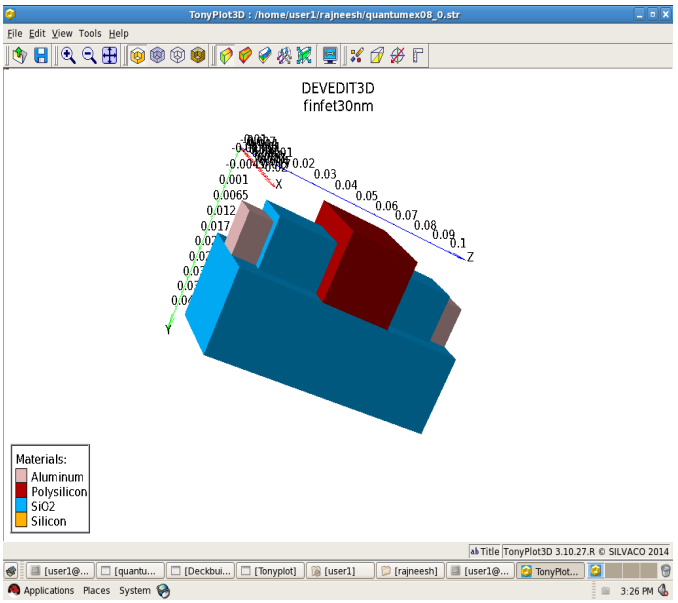

Figure 9. SOI FINFET Device

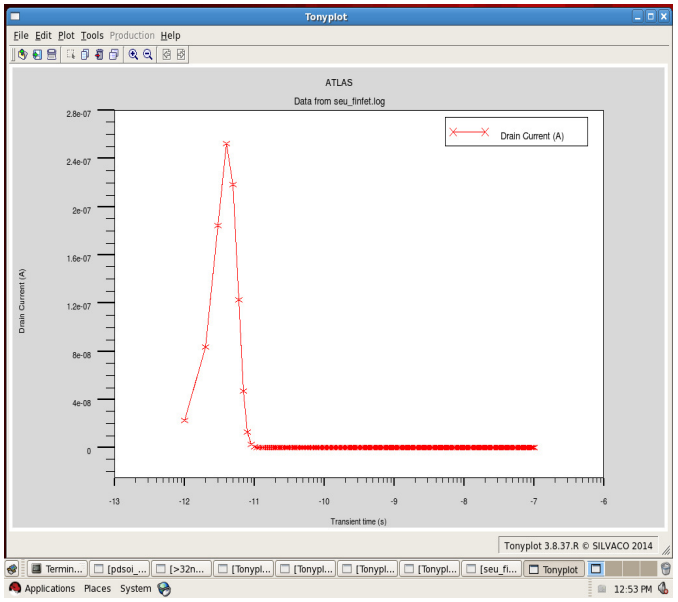

Fig. 10 Transient simulation of normal incidence in SOI FINFET

Again to show the effect of SEU on SOI device charged beam of particles is incident on drain terminal. The normal incidence is used in SOI device because the FIN height

(channel height) is small as compared to depth of substrate in 3D MOSFET. Incident angle of charged beam has not significant effect in SOI Structure because SOI structure has less volume of conductive region as compared to bulk devices. In case of FINFET only channel is conductive, rest at the bottom is Sio_2 which is insulator has not significant effect of charged beam. FIG. 10 shows transient simulation result of charged particle beam on SOI FINFET. Simulation results shows that very low drain current peak at 0.26 µA in case of SOI FINFET where as in MOSFET drain current peak at 0.35 mA.

Fig. 11 shows comparision of transient simulation in 3D MOSFET and SOI FINFET. Drain current peak is very low in case of SOI FINFET**.**

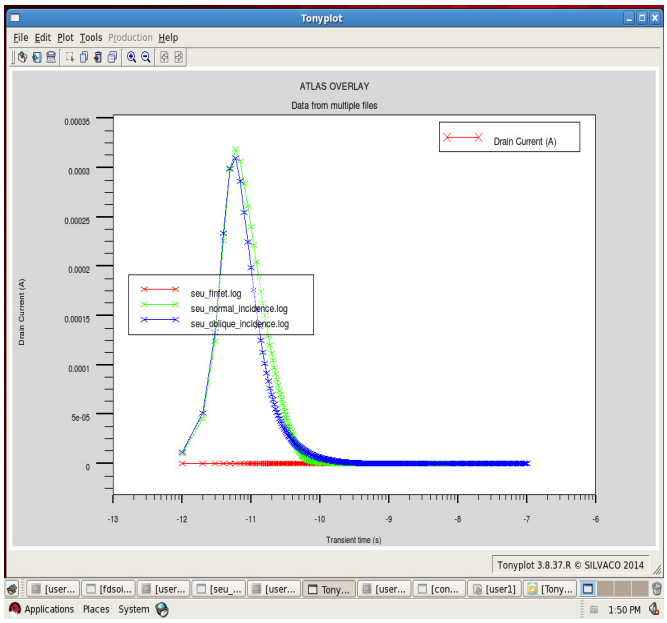

Figure 11. Comparison of Particle beam effects in 3D MOSFET and SOI FINFET

5. CONCLUSION

The 3D MOSFET is device simulated by using ATLAS simulator. Electrical response of the SEU in 3D MOSFET and SOI FINFET is studied. The variations of drain current due to fall of particle beam have been simulated. Simulation result shows that very low drain current peak at 0.26 µA in case of SOI FINFET where as in MOSFET drain current peak at 0.35 mA which is very low in case of SOI architecture. To mitigate SEU errors SOI architectures can be used and simulation result shows that SOI technology is right candidate for minimising SEU effects.

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