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TCAD Simulation of Nano Crystal Floating Gate EEPROM

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Abstract: **Nano crystal floating gate memory is considered a future nonvolatile memory because of its immunity to weak-point leakage in tunnel oxide and thus its superior scalability of tunnel oxide thickness and power consumption. Main feature of NCM is operating on a low voltage.**

1. INTRODUCTION

Flash memory device using nano crystals as floating gate have received attention because of its good memory performance and high scalability [1]. In nano crystals flash memory, charges are stored in nano crystals instead of a full poly-silicon floating gate. In conventional floating gate, if there is one defect across the tunnel oxide, all of the charges stored on the floating gate will leak back to channel or to the source/drain through the defect chain. The floating gate memory requires thick tunnel oxide to prevent the charge loss. The leakage problem can be eliminated by using semiconductor nano crystals memory structures [2]. The multi-nano crystal memory cell consists of a single FET device where a few electrons are stored in a layer of isolated nano crystal.

In this, we use technology CAD tools to study the Nano Crystal Memory (NCM) structure which is provide good characteristics such as, programming, erasing and data storage of non-volatile flash memory devices are examine through TCAD simulation using following the models: 1) Hot-carrier injection model to describe the writing process and 2) Fowler-Nordheim tunneling model to describe the charge removal or erasing process from the nano-dot in nano crystal flash memory devices.

2. DEVICE STRUCTURE

The multi-nano crystal memory cell consists of a single FET device where a few electrons are stored in a layer of isolated nano crystals. In nano crystal complementary metal oxide semiconductor (CMOS) compatible memories, a floating and isolated semiconductor nanometer size is coupled with channel of a MOSFET as shown in Fig. 1 [3].

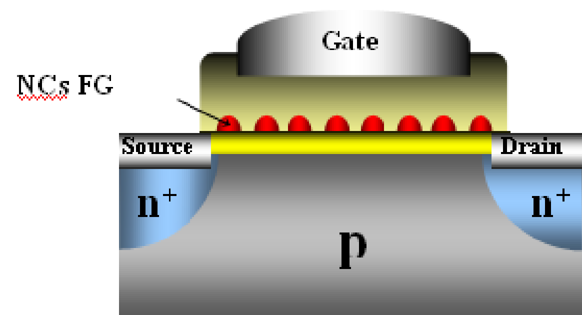

Fig.1 Device structure of nanocrystal memory [3]

A schematic cross section of the Nano Crystal device, based on a typical NMOS structure which is design in TCAD software is shown in Fig.2.

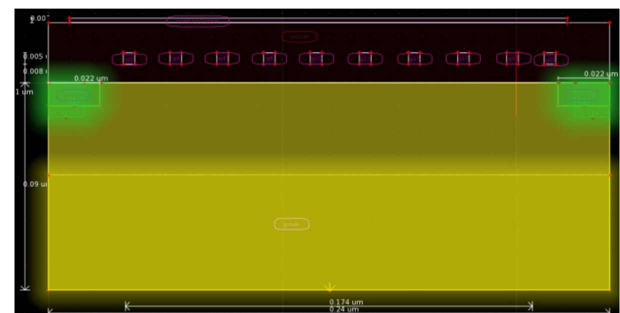

Fig.2 Geometry of Nanocrystal flash memory

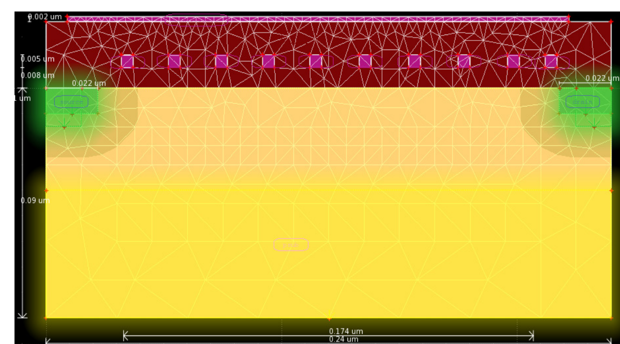

Fig. 3 Meshing File of NCM cell

The gate consists of an 8 nm tunnel oxide layer, poly-silicon nano crystal size are 5 nm, and a 13 nm blocking oxide layer between the channel and the poly silicon gate material with work function of 4.7eV. We take 10 nano crystal dots of 5 nm size. The meshing file of nano crystal flash memory is shown in Fig. 2, the material and simulation file shown in Fig.3 and Fig.4.

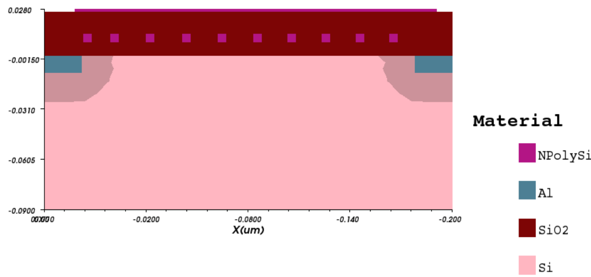

Fig. 4 Materials used in memory device

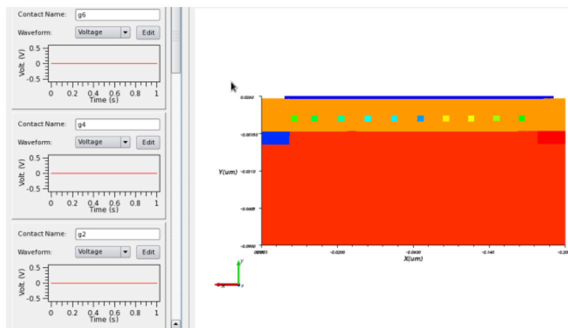

Fig.5 Simulation File of NanoCrystal non-volatile memory cell

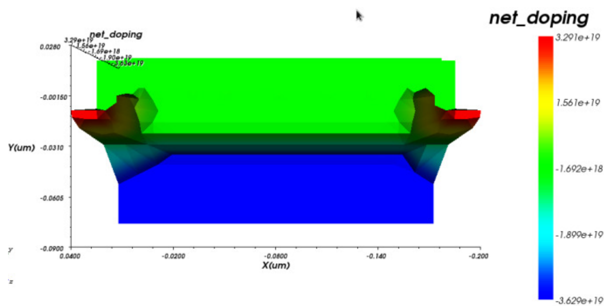

Fig. 6 Doping Profile of NCM cell

For programming Channel Hot Carrier Injection and Fowler-Nordheim tunneling process at the time of erasing was used. For the write process, a positive voltage is applied to channel inversion-layer electrons into the nano crystals. For the erase process, a negative voltage is applied to cause the electrons to tunnel back into the channel and accumulation-layer holes to tunnel into the nano crystal from the channel. The thickness of the blocking oxide is enough to block the electron and hole tunneling between the control gate and the nano crystal [2]. Hence tunneling across the control oxide is neglected.

It is assumed that the nano crystals are separated so that tunneling between nano crystals can be neglected [2].

3. RESULTS AND DISCUSSION

A) Channel hot electron programming

When the device turns on with applying high drain voltage, the electrons in the channel will flow from the source to drain region.

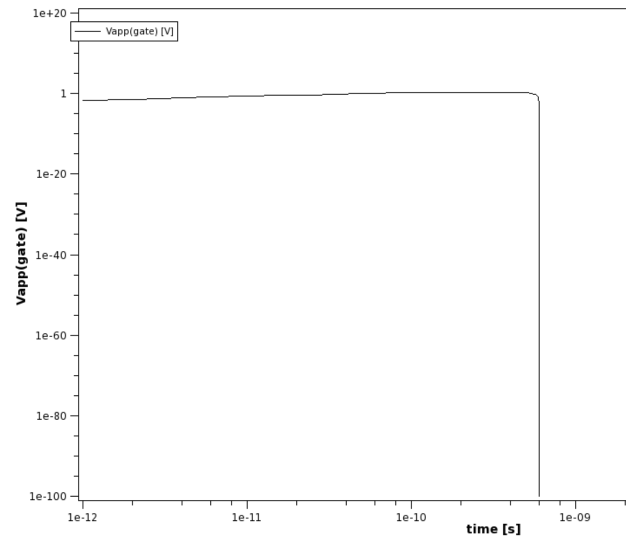

Fig. 7 potential during writing in a nanocrystal memory

At the pinch-off point of the device, the electric field starts to rise. The electrons are accelerated by high electric field, i.e. hot electron. Number of carriers gain sufficient energy to create impact ionization, which break down electron-hole pairs and produce the secondary electron and holes. Channel hot electron programming can be easily achieved in the nanocrystal cell [2, 3].

The hot electron current is high in the beginning of programming operation, but begins to drops as the negative charge injected onto the dot becomes significant and lowers the dot potentials, which is shown in Fig. 7. This cause to an increased threshold voltage decreases hot carrier injection.

B) Fowler-Nordheim tunneling erasing

Fowler-Nordheim tunneling is mostly applied for flash memory device erasing as control gate voltage increases with increasing oxide field and the potential barrier. Finally a detectable electron current starts to cross through the oxide. Currents through trapezoidal barriers are mention as direct tunneling currents, because electrons are injected directly into the polysilicon. The problem of tunneling through a trapezoidal barrier solved by the use of the WKB

approximation for tunneling from a metal electrode into vacuum by Fowler and Nordheim in 1928 [6].

The write and erase characteristics shown in Fig. 8.

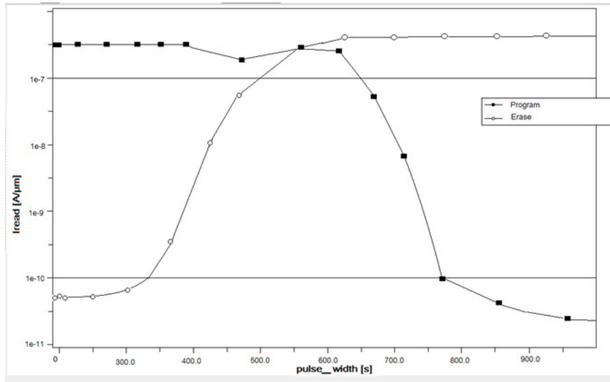

Fig. 8 Write and Erase waveform for NCM

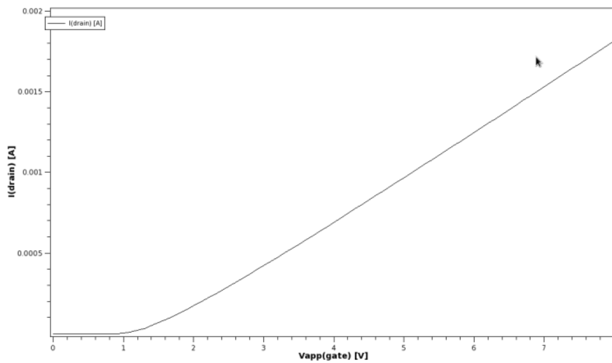

Fig. 9 Before Programming

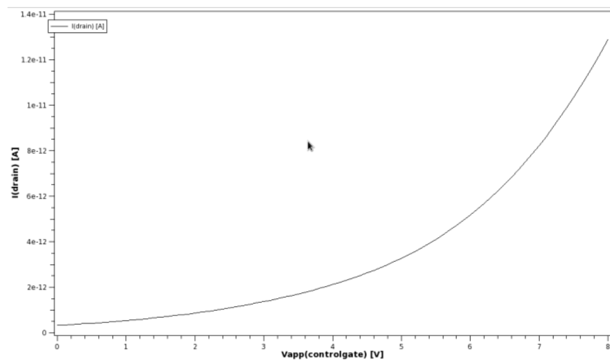

Fig. 10 After Programming

The tunneling current is high at the beginning of erase but decreases as the nano gate become less negative, thus reducing the field in the tunneling oxide as a result the threshold voltage decreases shown in Fig. 10.

4. CONCLUSION

The Nano Crystal Floating gate EEPROM is designed & simulated by using Visual TCAD software, write and erase operation of the memory cell is studied. The nanocrystal dots result shows the low voltage operation and reduce the size of tunneling oxide gives good performance and in future scaling will be at least 30 nm– 60nm.

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