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A Review on Junctionless Transistor - A Prospective sub-10nm Logic Device

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Abstract: **This paper reviews a new semiconductor device structure namely the Junctionless Transistor. This paper comprehensively presents the novel architecture of the Junctionless Transistor (JLT), which shows much promise in resolving the certain important issues related to the limitations of the conventional MOSFET and CMOS industry. The Junctionless Transistor has very low leakage currents, high on-to-off current ratio, better sub threshold slope, improved transconductance and less degradation of the carrier mobility with gate voltage and temperature than the classical transistors. Such a structure can be also referred to as Junctionless Gated Resistor (JLGR). They have lesser number of much simpler fabrication steps and hence less production cost than other contemporary logic devices.**

1. INTRODUCTION

The standard of human living has been greatly revolutionized by modern technologies. This is spearheaded by the advancement in semiconductor industry. The relevance of Semiconductor research is established by the recent Semiconductor Industry Associations' Reports [1] suggesting a worldwide turn over of an overwhelming $305.6 Billion sales in the year 2013, clear 4.8% increase over the figures obtained the year before. Moores' Law [2] has guided the trends in technology in his prediction of the technology node that is eapected to half in every eigheen months. This eapects the packing density of the integrated circuits to be doubled in one and a half years. But owing to voracious geometrical scaling [3] the semiconductor device dimensions are nearing the physical limits [4,5] such that they can not be further scaled down without adversely affecting their performance. Thus the progress of the semiconductor inductry is on the verge of stagnation owing to the limitations that have been ushered in from various technological bottle necks. Efforts are now being made to get around the problem and reach the goals set up by the industry through the International Technology Roadmap for Semiconductors [6]. Such efforts have seen various research groups exploring novel device architectures, starting from the Strained Silicon Technologies [7] spanning the Silicon-on-Insulator (SOI) structures [8], the multi-GATE architectures like the Fin-FETs [9-13] and other advanced Gate Engineered Transistors of late [14,15].

The main issues which stand in the way of success of the semiconductor devices in the deep sub-micron regime, (order of 10nm and below), are the sharp gradient in doping profiles, thermal budget issues for processing, various short channel effects like drain induced barrier lowering, punch through,etc. and finally the sub-threshold characteristics of such small dimensional devices. As predicted by ITRS 2012 reports, the geometrical gate length is stipulated to reach 9nm at around 2016. At such a small gate length the quantum mechanical effects like carrier quantisations become predominant. The source-substrate and drain substrate junction formation in small scale devices become very difficult as it requires sharp doping density gradient which causes thermal budgeting issues. The performance of such small scale devices deteriorate due to the various detrimental short channel effects [16]:

- drain-induced barrier lowering
- punch through
- surface scattering
- velocity saturation
- impact ionization
- hot electron effect

The narrow width effects also become predominantly large, bringing device performance metrices below tolerance limits. With the complexity of the device architectures, process variations and corresponding complexities increase manifold. Therefore the fabrication of such novel device structures involves costly equipments leading to rise in batch fabrication and production cost per chip.

Hence simpler and novel device structures may prove to be potent enough to eliminate all the above drawbacks and perform well in the sub 10nm regime.

2. PHYSIC OF CURRENT CONDUCTION IN JUNCTIONLESS TRANSISTOR

It has been reported by J P Colinge et.al [17,18] the physics of the Junctionless Transistor (JLT) is very different from that of the MOSFET. Current conduction is a bulk phenomena in JLT. The normally on-channel conducts during the on-state when bias is applied across source and drain**.** The gate voltage induces depletion region in the channel to turn off the current. The channel depletion constricts the cross section of the channel and reduces the current flow. Finally the channel is pinched off. Since current conduction in JLT is a bulk phenomena, the channel needs to be made much thin for the gate voltage to be able to turn off the transistor. Also the channel region has to be highly doped in order to turn the channel on fast. The conduction phenomena in JLT is similar to that of the Field Effect Transistor.

3. REVIEW WORK

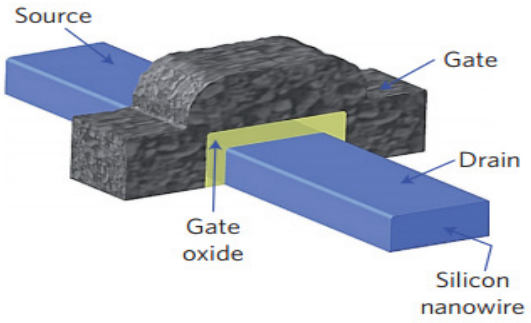

Figure 1: Junctionless Transistor [17]

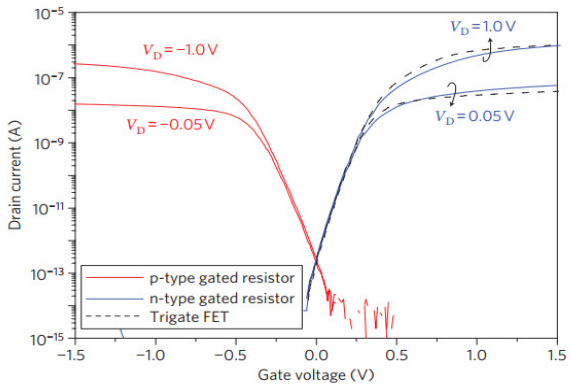

Figure 2: Current Voltage Charecteristics [17]

J P Colinge et.al in a paper entitled, ”Nanowire transistors without junctions” [17] have established a novel MOS-structure, namely the Junctionless Transistor, that addresses all the above limitations as the physical channel length scales down to the order of 10nm. This device has been patented by the group [18]. This structure can be also referred to as Junctionless Gated Resistor. It has simpler and less number of fabrication steps than the conventional MOSFET. Hence the fabrication cost is less.

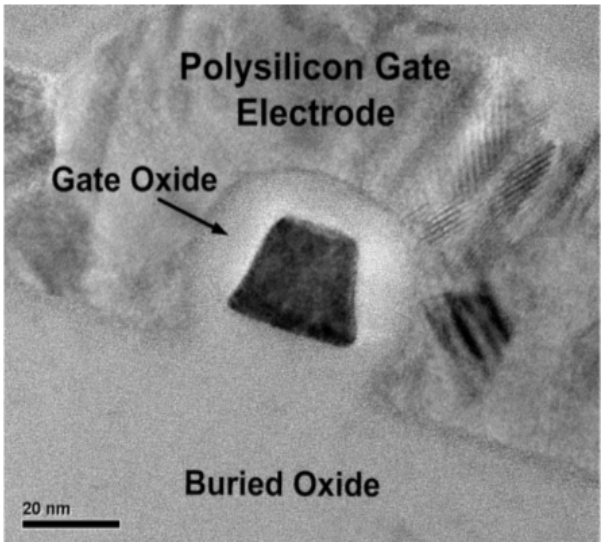

Figure 3: TEM cross section of a junctionless nanowire transistor[19].

Dr. A Kranti, J P Colinge and their research group have detailed the design guidelines of such a structure [19]. The Analog behaviour of Junctionless Transistor at temperatures ranging form 100K to 473K is presented by Dr. A Kranti, Prof. J P Colinge and their group [20]. In the paper entitled “Junctionless Multiple-Gate Transistors for Analog Applications” [21] the authors have pointed out that the device shows better analog properties than their conventional inversion mode counterparts. The ITRS prediction of increase in operation speed and improved drive current for devices with strained Si in n-type and p-type junctionless trasnsistor and strained channels are supported in the paper [22]. High temperature performance [23,24] and short channel effects [25,26] of such a structures have also been investigated. Dr. A Kranti in [27] has shown the huge potential of Junctionless MOSFETs for Ultra Low Power analog/RF applications. He has also concluded that such a structure requires simpler fabrication process as there is no need for any source-drain region formation and related engineering. For channel length of as small as 16nm Ge bulk nanowire junctionless transistor is shown to have a subtheshold slope of 77mV/decade and drain-induced-barrier-lowering of 70mV for an on-off current ratio of 1.1 × 10 5 as has been shown in [28] . Papers [29,30] establish the simplicity of fabrication steps of Junctionless

Transistors as opposed to that of the conventional CMOS process flow. Junctionless Transistor based inverter has also been proposed which shows high on off current ratio and better short channel behaviour in 10nm technology node and even beyond. Research is also being pursued to fabricate Junctionless Transistor based Nanoscale Appplication Specific Integrated Circuits [31] . Many literatures [32-34] on the drain current models and compact models of the junctionless transistors are also being reported.

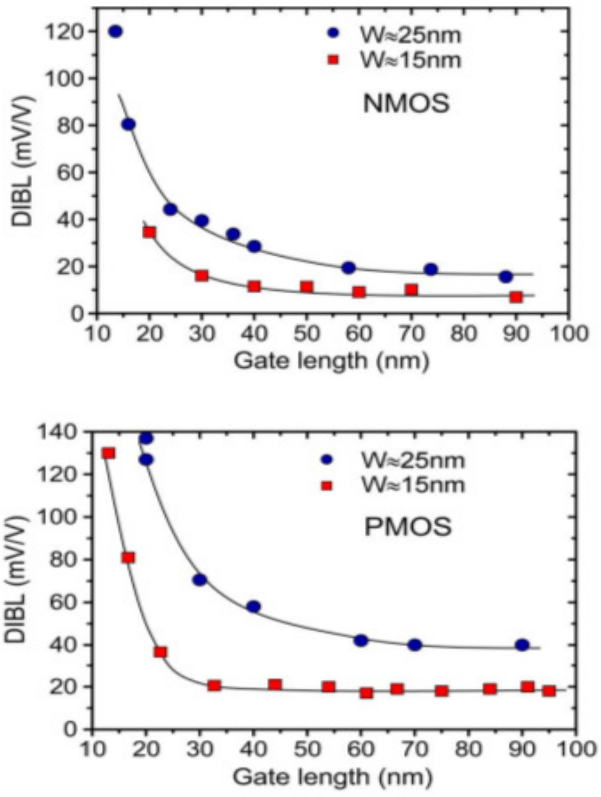

Figure 4a and b:Measurements of DIBL [36] as a function of gate length for both NMOS and PMOS trigate JL NW MOSFETs.

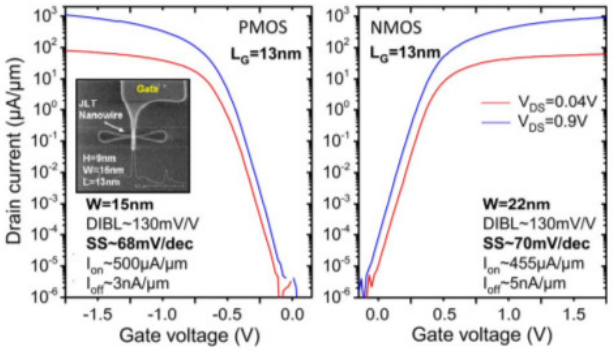

Figure 5:I_D-V_{GS} Charecteristics[36]

Figure 4a and b shows measurement of DIBl and Figure 5 shows I_D-V_{GS} Charecteristics as given in [36] for trigate junctionless nanowire transistor whcih shows better performance at 13nm node point for high K/metal gate stack.

4. CONCLUSION AND DISCUSSION

Many research groups have considered Junctionless Transistor(JLT) as a potential research domain and their contributions have provided enough evidence to consider JLT as a future logic device.

Better high temperature performance, improved shorth channel behavior and simple fabrication step makes it an automatic choice.

5. FUTURE SCOPE

With latest research establishing the superiority of the JLT over contemporary alternatives, the compact modelling of JLT is the most important future scope. SPICE based compact model developement for such a structure can help in the circuit implementation and realise the Moore's Law for future semiconductor industry.

Use of non-silicon semiconducting materials in such a structures may result in improved performance metrices. High-K gate stack has already been investigated but GaAs channel JLT needs to be studied to find out if it shows better high frequency responses and low power performance of non-silicon devices may also be further looked into.

6. ACKNOWLEDGEMENT

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