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Simulation of Double Gate MOSFET at 32 nm Technology Node Using Visual TCAD™ Tool

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Abstract: **With scaling MOSFET into sub 50 nm node there is a marked increase in the Drain induced barrier lowering, channel length modulation, gate leakage and increase in sub threshold slope all these effects are attributed to decreased gate coupling to the channel. Traditional technique to increase the gate coupling was through increasing gate capacitance by reducing the gate oxide thickness, this reduced oxide thickness caused large increase in gate leakage current thereby increasing the static power consumption, of suggested solutions is use of high K materials like hafnium oxide in place of silicon dioxide. Use of such materials have compatibility issues with existing silicon processing technology. It is suggested that a greater gate coupling can be achieved through introducing an additional gate below the channel. Such a device architecture is expected to help in improving the MOSFET performance at 32 nm node. Threshold voltage, Drive current, gate leakage current, ION - IOFF ratio, DIBL and transconductance of the simulated device was extracted.**

1. INTRODUCTION

More than 30 years, the MOSFET have continually been scale down in size in channel length from micrometers to sub micrometers and then sub micrometers range to nanometer following Moore's Law. These nanoscale devices have a significant potential to revolutionize the fabrication, integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS [1]. For the past four decades, the cost-per-function and the performance of integrated circuits have been dramatically improved by successful scaling of planar bulk Si CMOS devices. However, as the gate length (Lg) decreases, the capacitive control of the channel potential by the gate becomes more difficult [2].

Instead, the source and drain influence significantly the channel potential, resulting in severe short channel effects (SCE), such as increased off-state leakage current (I_{OFF}), threshold voltage (V_T) roll-off, i.e., smaller V_T at shorter gate length (L_g), and drain-induced barrier lowering (DIBL), i.e. smaller V_T at higher drain voltage (V_d) due to modulation of source-channel potential barrier by the drain voltage.

In order to suppress the SCE in bulk devices, other parameters have been scaled down together with gate length (L_g), such as the gate oxide thickness (T_{OX}), the gate-controlled channel depletion width (X_d) and the source/drain junction capacitance (X_j) [2].

A thin gate oxide increases the capacitive control of the channel by the gate. Therefore, the influence on the channel by the source/drain becomes relatively small. At the same time, more inversion charges are induced by T_{OX} scaling, resulting in higher on state drive current (I_{ON}). The size reduction of the device makes great improvement to MOSFET operation [2].

The future technology trend predicted by ITRS (International Technology Roadmap for Semiconductors), physical dimensions and electrostatic limitations faced by conventional process and fabrication technologies will require the dimensional scaling of complementary metal-oxide-semiconductor (CMOS) devices within the next decade. To enable future technology scaling, new device structures for next-generation technology have been proposed [3].

Nowadays, many researchers have been done to improve the performance of the device in obtaining higher speed, low power consumption, low cost and smaller device. There are many new techniques that are study in the present time to improve the MOSFET from there one of the technique is Double Gate MOSFET. The main idea of a Double Gate MOSFET is to control the silicon channel very efficiently by choosing the silicon channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to reduce the short channel effects and leads to higher currents as compared with a MOSFET having only one gate. The larger the number of gates provides the better electrostatic control of the channel [4].

The double-gate (DG) MOSFET is a favorable structure for scaling CMOS into the sub-50 nm gate length (L_g) regime because of its excellent suppression of short channel effects (SCE) for a given equivalent gate-oxide thickness [5].

2. OPERATION OF DOUBLE GATE MOSFET

The double-gate MOSFET is a latest device structure that is a best candidate for replacing conventional bulk MOSFETs

beyond the 50-nm technology node [5]. Fig.1 shows the geometry of double gate MOSFET.

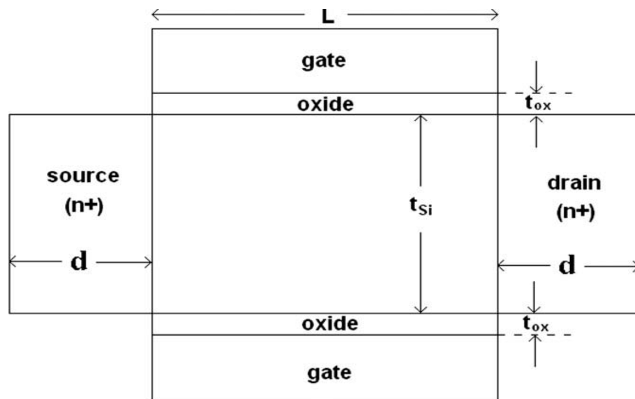

Figure1. Structure of double gate MOSFET [1]

The DG MOSFET can be regarded as an evolution of the regular MOSFET structure, with a second gate placed below a thin body in which the channels are formed. In the most effective DG MOSFET implementation, both gates are electrically connected (driven by the same voltage) or they can be independent, and the top and bottom gate dielectrics have the same thickness [5].

The most common mode of operation of the DG MOSFET is to switch the two gates simultaneously. Another use of the two gates is to switch only one gate and apply a bias to the second gate to dynamically alter the threshold voltage of the FET. In this mode of operation, called "ground plane" (GP) or back-gate (BG) [6].The sub threshold slope is determined by the ratio of the switching gate capacitance and the series combination of the channel capacitance and the non switching gate capacitance, and is generally worse than the DG MOSFET. A thin gate dielectric at the non switching gate reduces the voltage required to adjust the threshold voltage and preserves the drain-field shielding advantage of the double-gate device structure [7]. Due to the presence of two gates each gates control the half of the device and then operation is completely independent of the other. Then the total current of the device is equal to the sum of the current of the two channels which is in device by applying the gate voltage. The relative scaling advantage of Double Gate MOSFET is about two times. The performance of symmetric version of Double Gate MOSFET is increase by the higher channel mobility as compared to bulk MOSFET [8]. Since the average electric field of the channel which is formed in the device is lower which decrease the interference roughness scattering according to universal mobility model [9].

3. FEATURES OF DG MOSFET

The salient features of the DG MOSFETs are

1. The Control of short-channel effects by device geometry as compared to bulk MOSFET, where the short-channel effects are controlled by doping [10].
2. A thin silicon channel leading to tight coupling of the gate potential with the channel potential [10].

These features provide potential DG MOSFET advantages that include

1. Reduced 2D short-channel effects leading to a shorter allowable channel length.
2. A sharper sub threshold slope which allows for a larger gate overdrive for the same power supply and the same off current [6].
3. Better carrier transport as the channel doping is reduced or the channel can be undoped.
4. The potential advantages in Double Gate MOSFETs allows for higher current derive capability.
5. The gate capacitance is also double due to the presence of double gate in device (per device areas).

4. TYPES OF DG MOSFET

As far as the electrostatic of the Double Gate MOSFET is considered it can be design as SDG and ADG

There are two types of DG MOSFETs
1. Symmetric DG MOSFETs
2. Asymmetric DG MOSFETs

These are describing as follows:

1. Symmetric DG MOSFET in which the both the gates have identical material or work function as shown in fig 2. The both gate tied with same bias. At ON-state, the two conductive channels (inversion layers) are formed on the two side of silicon body for the SDG device. These channels conduct at the same time [8].

In addition the SDG device shows higher carrier mobility due to its lower transverse electric field as compared to the ADG device [3]. The structure of symmetric double gate MOSFET is as shown in fig 2.

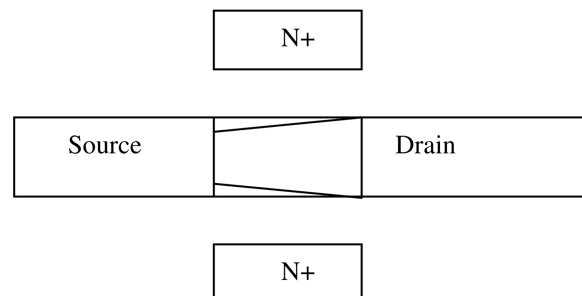

Figure2. Symmetric DG MOSFET

2. Asymmetric DG MOSFET in which both the gates have different material or work functions as shown in fig 3. These have two different work function of both the gates. DG MOSFET switching can be obtained by applying different voltage at both the gate [2]. An only one channel is formed for the ADG device unless the operation voltage is extremely high to form the other inversion layer near the P+ gate. The threshold voltage of an ADG MOSFET can be adjusted by changing the body thickness (T_{si}) and/or the gate-oxide thickness (T_{ox}), without the need for exotic gate materials.

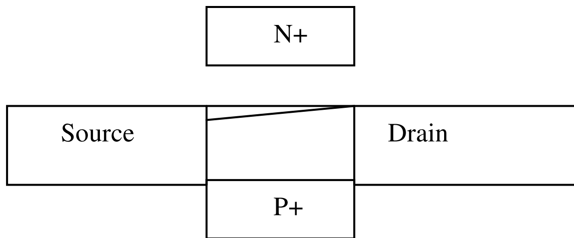

Figure3. Asymmetric DG MOSFET

5. DESIGN AND MATERIAL

To design a DG MOSFET at 32nm technology. First we make geometry of the Double Gate MOSFET in which we define various region which are Substrate, Gate Contact (G), Drain (D), and Source (S). Then doping is done to drain, substrate and source regions and material of various regions are defined which are shown in Table 1 below. The material used gate contact is poly silicon and rectangular gate region lies on top of the substrate separated by a thin dielectric with thickness (T_{OX}). Table 1 shows regions and materials used in simulation of device. Table 2 shows doping and profiles used in device.

Table 1. Regions and Material used 32nm device

Region	Material
Substrate	Silicon
Source	Aluminium
Drain	Aluminium
Gate	N poly silicon

Table 2. Design parameter of 32nm Device

Device Design Parameter	
Channel thickness (T_{si})	11 nm
Gate oxide thickness(T_{ox})	2 nm
Gate Length	32 nm
Doping conc.(N-type)	$2{\times}10^{21}$ cm^{-3}
Doping conc.(P-type)	$2{\times}10^{15}$cm^{-3}

6. RESULT AND DISCUSSION

To design the geometry of 32nm DG MOSFET we use Visual TCAD tool which is a device simulation tool.

The figure 4 is as shown the geometry of DG MOSFET

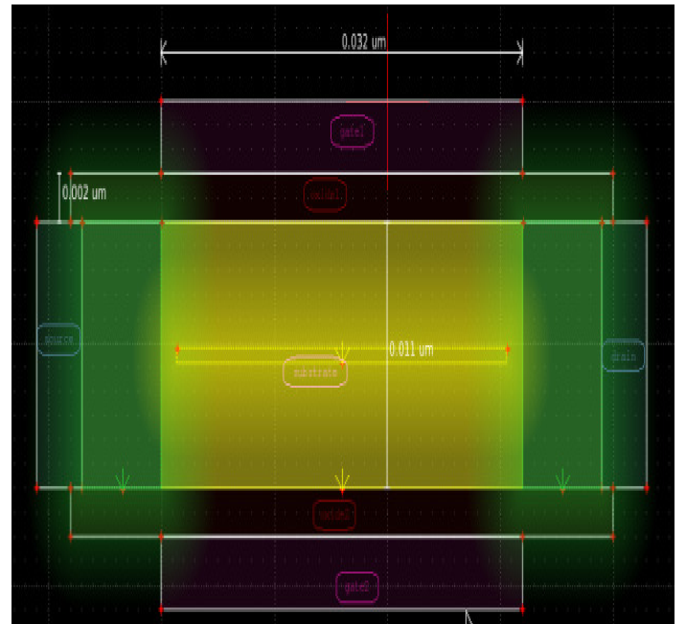

Figure 4. Geometry of 32nm DG MOSFET

In Fig 5 meshing file of 32nm double gate MOSFET. Fig. 6 shows the regions of device.

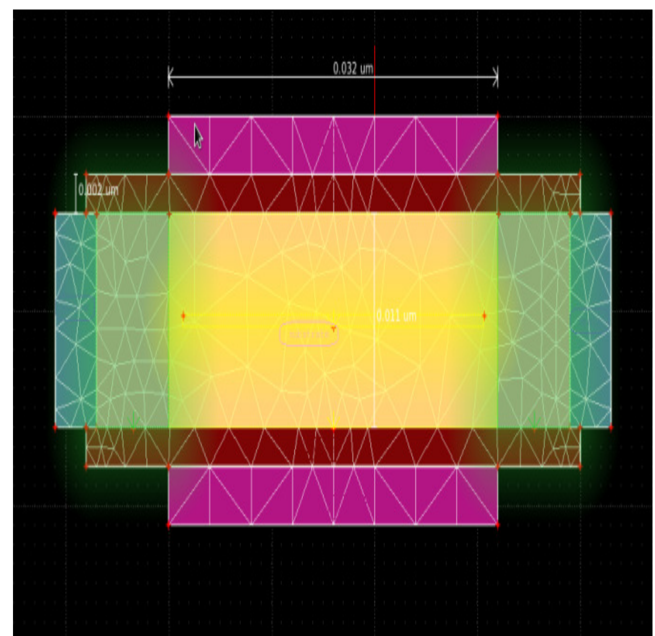

Figure 5 Meshing file of the device

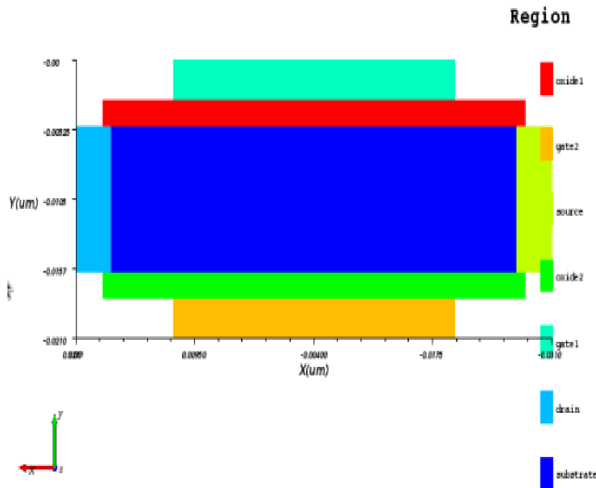

Figure 6 Regions of 32nm DG MOSFET

After the simulation we get the I_D versus V_{GS} plot. Fig 7. shows that I_D versus V_{GS} curve for the device. By this curve, the value of threshold voltage (V_T) can be found out. The minimum voltage at which channel starts creating is called threshold voltage. Here drain voltage $V_D = 0.3V$ is applied for this device. Figure 8 show the I_D versus V_{GS} of different back gate voltages for 32nm DG MOSFET. Here gate2 is at fixed bias where gate1 is ramped from 0V to 1.2V. As shown in the figure drain current is begin to rise as rise in the gate1 voltage after threshold voltage, multiple curves are shown for different back gate voltages. Here in the figure shows that V_T is decreases as the back gate voltage increases. The back gate adjusts the V_T. The curve is plotted using Visual TCAD ™ with GENIUS simulator. From figure 7 it is observed that the V_T of 32nm device is 0.27V.

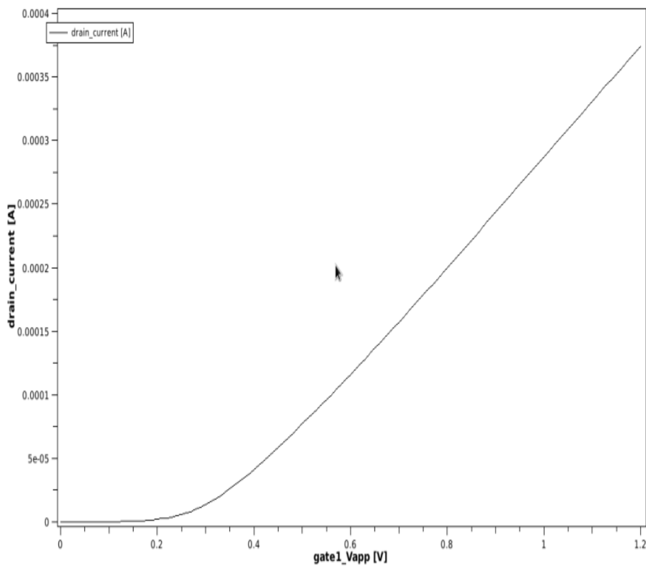

Figure 7 I_D versus V_{GS} curve

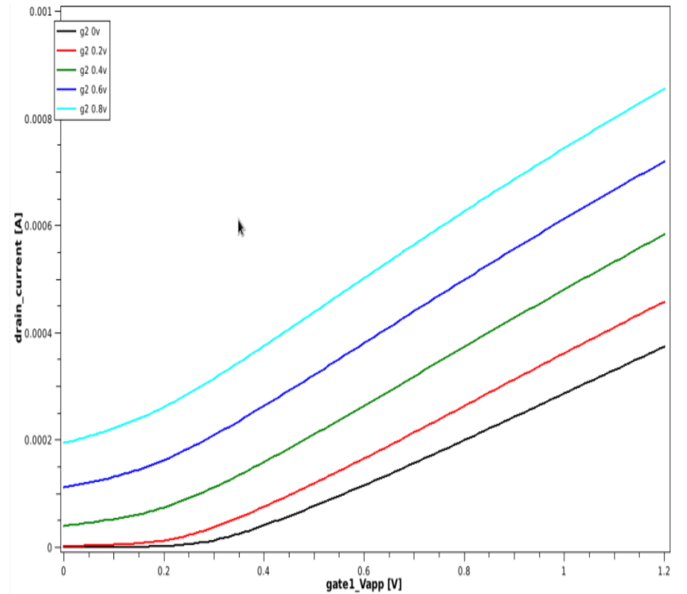

Figure 8 I_D versus V_{GS} curve at diff. back gate voltage

The curve betveen I_D versus V_{DS} is obtained at constant V_{GS}. By this curve the value of transconductance is obtained. Figure 9 shows the curve between I_D versus V_{DS} at different values of V_{GS} while back gate is kept at fixed voltage. The value of transconductance is found is $3.5\times10^{-4}\ \Omega^{-1}$.

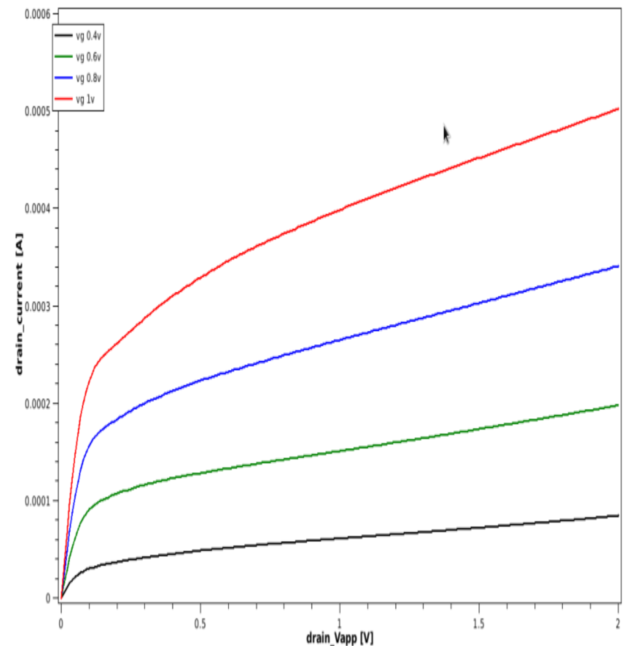

Figure 9. I_D versus V_{DS} curve at different V_{GS}.

The curve between I_{ON} versus I_{OFF} ia as shown below in fig 10. From graph we obtain the leakage current and we also obtain I_{ON}-I_{OFF} ratio.

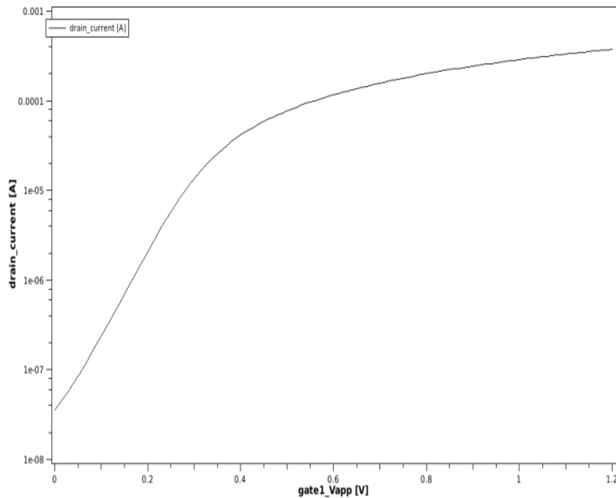

Figure 10. I_{ON}-I_{OFF} current

The electron density of various region of 32nm double gate MOSFET is as shown in fig 11

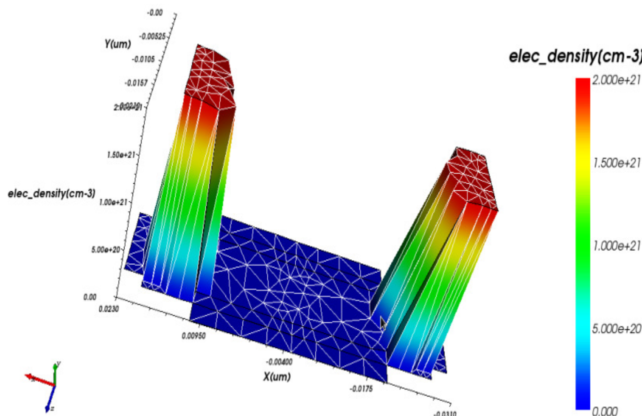

Figure 11. Electron density in 32nm device

Table 3. Simulation result of 32nm DG MOSFET

V_{DD}	1.2v
Threshold voltage (V_T)	0.27v
Drive current (I_{ON})	0.000374223A
Leakage current (I_{OFF})	3.548×10^{-8}A
I_{ON}-I_{OFF} Ratio	1.05×10^{4}
Transconductance (G_{DS})	$3.5\times10^{-4}\Omega^{-1}$
DIBL	7.78×10^{2}

7. CONCLUSION

As we observe the simulation results of 32nm DG MOSFET is that it gives the 0.27V threshold voltage at V_{DS} 1.2V. This device is reduced the drain induced barrier lowering (means small variation of threshold voltage at low and high drain voltage) and better I_{ON}-I_{OFF} ratio is achieved. This device is useful to overcome the short channel effects.

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