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Simulation of 6T SRAM at 90nm and 180nm Technology and Study the Effect of Scaling on Read and Write Operation

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Abstract: **There is a need for electronic devices for communication, computing, entertainment, automotive, and other applications where MOS ICs have fulfilled the expectation with rapid improvement in cost, speed and power consumption. In this paper, a 90 nm and 180 nm SRAM Cell was designed and simulated to study its read and write operation characteristics using Visual TCAD using mixed mode simulation. From device level construction of MOSFET an approach for CMOS device construction is developed further mixed mode structure of 6T SRAM Cell is developed.**

1. INTRODUCTION

Memory arrays are an important part of the processors. The memory arrays are made of many SRAM cells. Each cell store a single bit of data. In order to store sufficient amount of data an array of cells is used. These SRAM cells are available in many configurations depending upon number of transistors used. In order to increase the density of the manufactured chips, the channel length of the devices is being reduced. This in turn leads to decrease in power dissipation.

The rapid scaling of CMOS device achieves higher density, improved performance and lower power consumption. Transistor delay time also decreased as the technology results in doubling of microprocessor performance in every two years. To keep the power consumption under control, the supply voltage has been scaled down as the threshold voltage and the transistor has to be scaled to achieve high performance. The threshold voltage scaling results in increasing of the sub threshold Leakage Current[1]. Since the 1960s the cost of one bit of semiconductor memory has reduced 100 million times and this trend continues further. The cost of a logic gate has undergone a similarly dramatic reduced. This rapid rice drop has stimulated new applications and semiconductor devices have improved the way the people carry out just about all human activities.

2. OPERATION OF 6T SRAM CELL[2]

6T SRAM cell refers to memory cell which uses six- transistor to store one bit of information. The figure 1 below shows basic 6T SRAM cell.

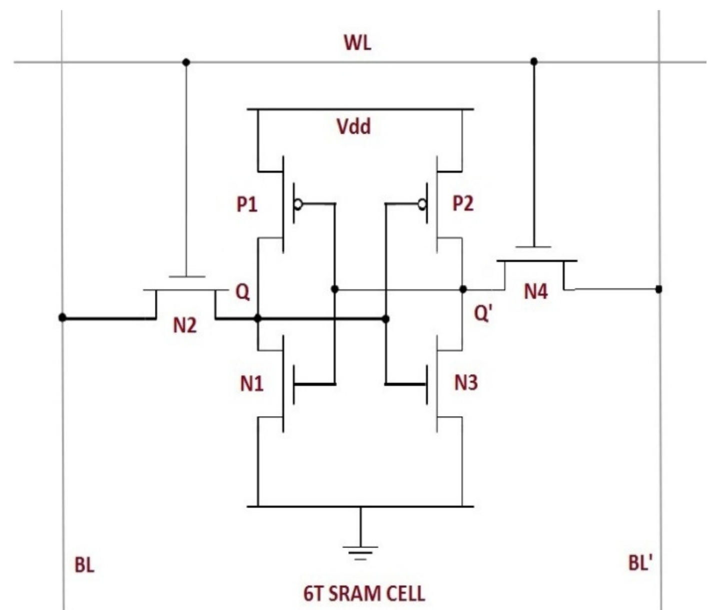

Fig. 1 6T SRAM Cell [2]

The data to be stored is applied to Bit Line BL' and its complement to BL. Q and Q' are two storage node. N2 and N4 are two access transistors. P1 and P2 are the pull up PMOS transistors and N1 and N3 are two pull down NMOS transistors. P1, N1 and P2, N3 are two pairs of cross coupled inverter. The Word line WL is censure for keeping the cell in active or standby mode. Its value will decide whether access transistors switch on or off[5]. During read operation, the data stored is read from two complementary Bit lines. Word line is deactivated in the hold state and no activity is performed in the cell in this mode. The data would remain as such. VDD is the supply voltage. Scaling of devices leads to reduction in the supply voltage and hence power decreases but stability of the cell decreases

1. Design and Materials

To design a SRAM Cell we first design a NMOS at 90 nm technology. Firstly we design geometry of the MOS in which

we design various region like Substrate, Gate Contact, Drain, and Source. After this doping is done in drain, substrate and source regions and material and mesh size of various regions are defined which are shown in Table 1. The material used in gate contact is poly silicon and for gate and substrate contact aluminium is used and rectangular gate region lies on the top of the bulk separated by a thin layer of silicon oxide dielectric with thickness T_{OX}. Table 1 shows regions and materials used for simulation of device. Table 2 shows doping and profiles used for device simulation.

To reduce various short channel effects an implant of concentration somewhat higher doping is done in channel. Also to curb Hot Carrier Effects LDD are used.

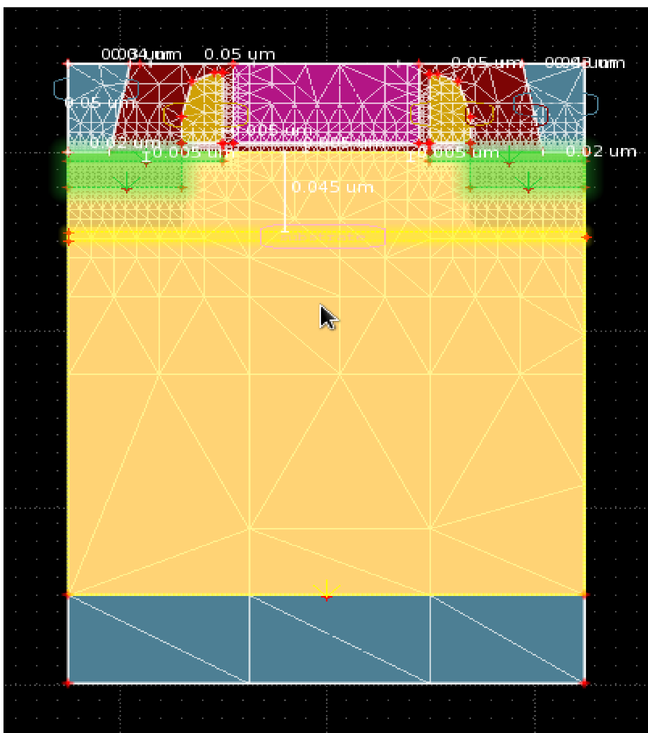

Fig 2 Device Structure of 90 nm NMOS

In Fig 3 Electron density of various regions in NMOS are shown in figure. The bulge that is shown in Fig 3 shows drain and source regions. Figure 4 Shows that I_d vs. V_{ds} curve of NMOS device. From this curve, the value of threshold voltage (V_{th}) can be found out. The minimum voltage at which channel starts developing is called threshold voltage. Here drain voltage V_d = 1V is used for this device. When $V_g < V_{th}$, the current Id =0 but the current start increasing when $V_g > V_d$. With a small value of V_{ds} applied it is possible to find out the effect of an increase gate voltage. Figure 8 show the families of Id versus V_{gs} curve for NMOS. The curve is created using Visual TCAD with GENIUS simulator. From figure 5 it is seen that the V_{th} of NMOS device is 0.256V

Table1. Regions and Material used in NMOS

Region	Material	Max Mesh Size (μm)
Substrate	Silicon	0.5
Substrate Contact	Aluminium	0.5
Spacer1	Nitride	0.5
Spacer2	Nitride	0.5
Drain	Aluminium	0.5
Source	Aluminium	0.5
Gate	N Poly Silicon	0.5
Oxide	Sio_2	0.5

Table 2. Doping Profile

Name	Profile	Type	DOPING	X/Y Ratio	Char. Length
Body	Uniform	Acceptor	5e+16	-	-
Implant	Gaussian	Acceptor	1e+18	1	0.005
Channel	Gaussian	Acceptor	1e+18	1	0.005
LDD_S/LDD_D	Gaussian	Donor	1e+20	0.05	0.01
Drain/Source	Gaussian	Donor	2e+19	1	0.002

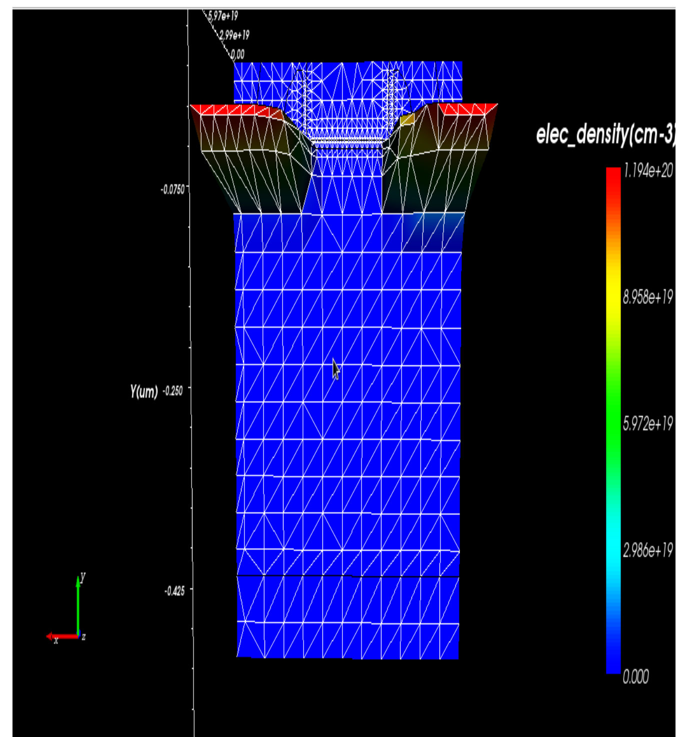

Fig.3. Electron density in NMOS

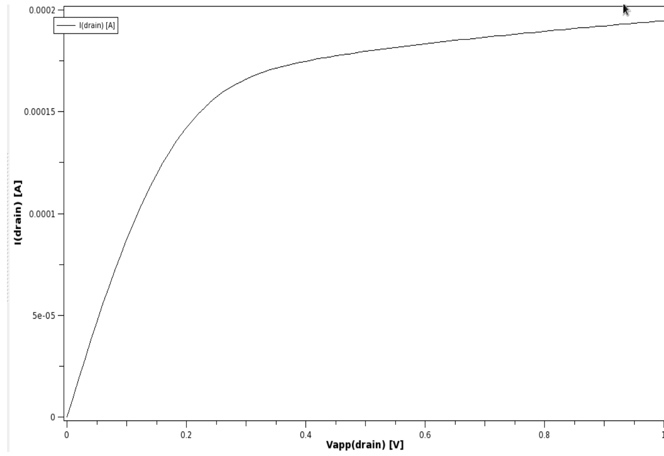

Fig4. I_d-V_{ds} curve of NMOS

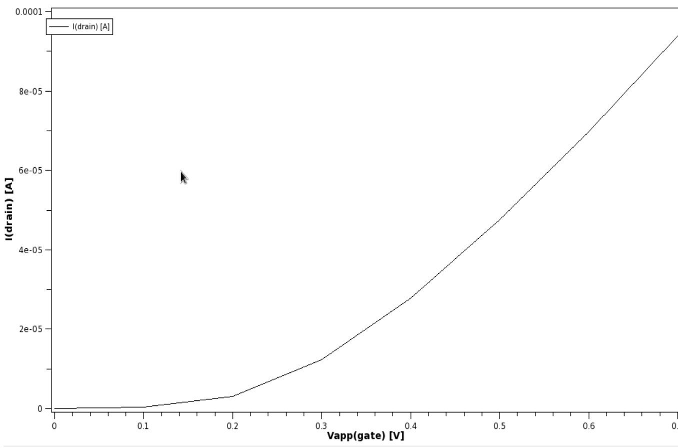

Fig5. I_d-V_{gs} curve

Similarly design of NMOS at 180 nm has prepared.

3. SIMULATION OF SRAM CELL AT 90NM

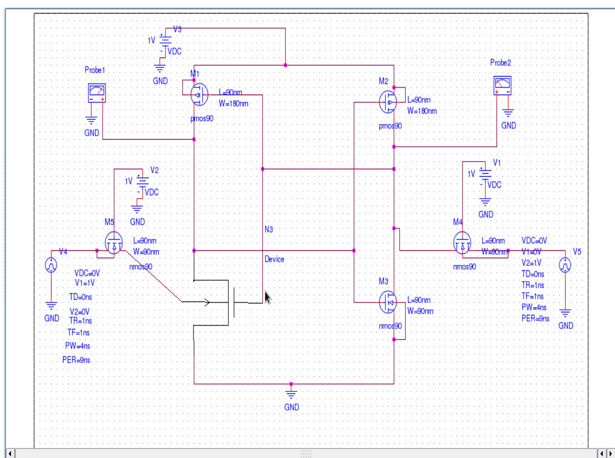

Fig6. 6T SRAM Cell write operation

Mixed Mode circuit simulator is a circuit simulator that includes physically-based devices in addition to compact analytical models. In fig6. We use a NMOS that is designed at device level at 90nm. Fig 8 consist of two access transistor and two cross coupled CMOS inverters connected back to back .Probe are used for finding value of the voltages

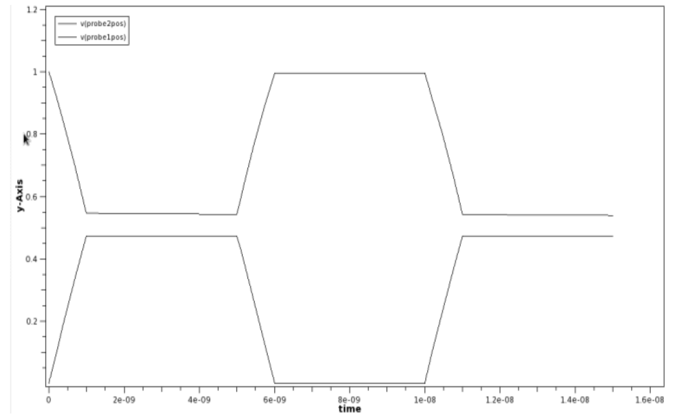

Fig7. Write curve of 6T SRAM

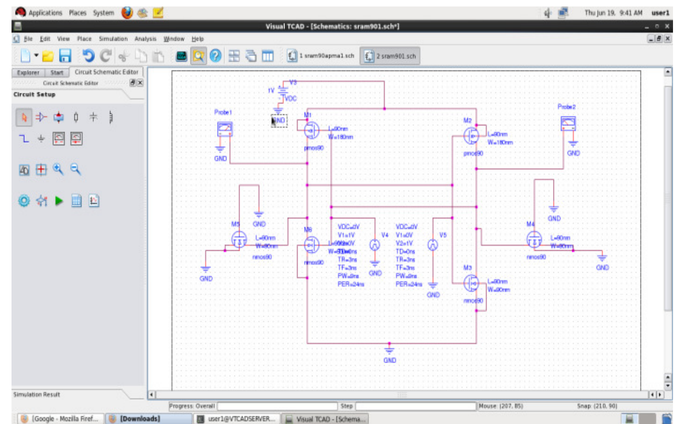

Figure8. 6T SRAM circuit for read operation

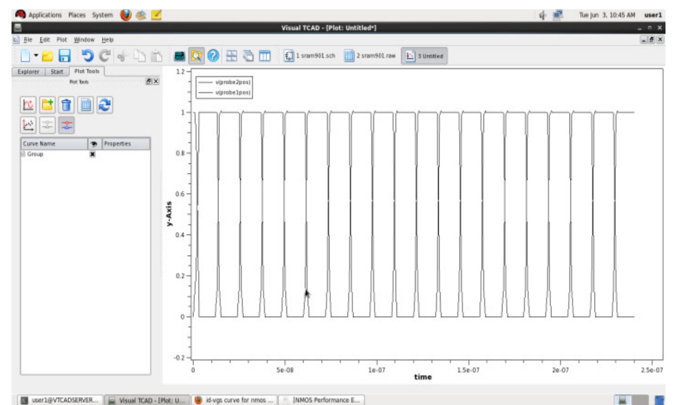

Figure9. Read curve 6T SRAM

The read and write waveform of 6T SRAM cell are shown in Figure 9. During the read operation, output is taken from read path and word line remains active high during write operation, the input is applied at Bit lines and WL is used. During hold the WL remains off and cell is in idle state

4. SIMULATION OF SRAM CELL AT 180NM

In Fig6 We use a NMOS that is made at device level at 180 nm. Here this consist of two access transistor and two cross coupled CMOS inverters connected back to back .Probe are used for finding value of the voltages

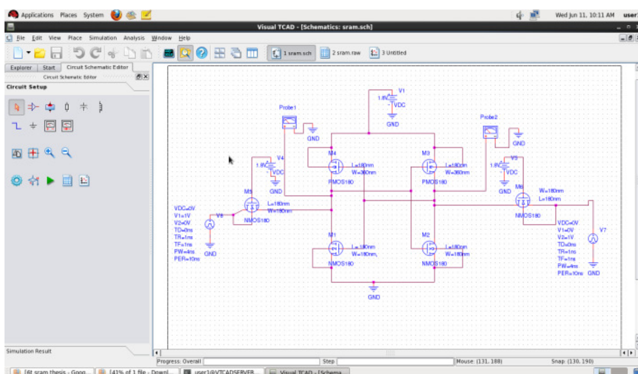

Fig10. 6T SRAM write operation at 180nm

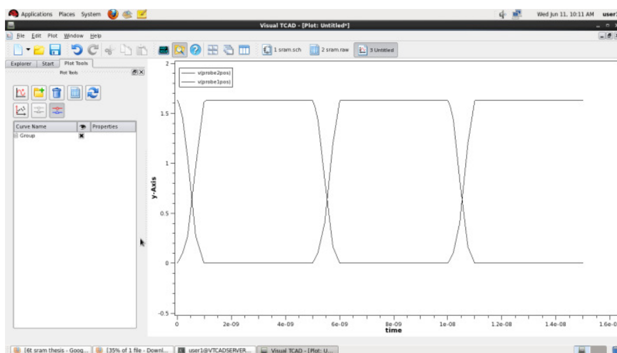

Fig11. Write curve of 6T SRAM

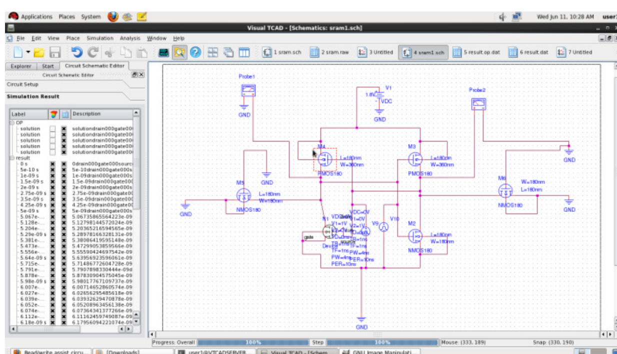

Figure11. 6T SRAM circuit for read operation

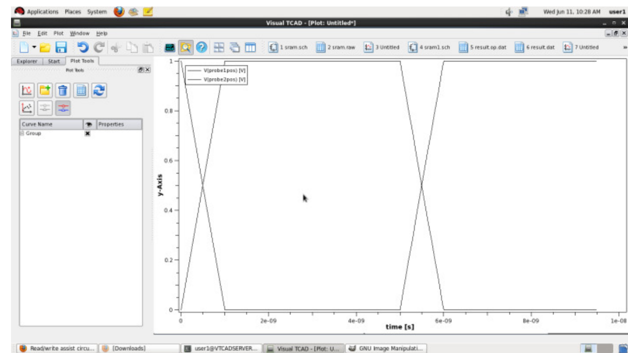

Figure12. Read curve 6T SRAM

The 3-D structure of 6T SRAM can also be designed using GD2Mesh geometry constructor.

Device Level Implementation in this is done using Visual TCAD. GENIUS simulator is used for 3D simulation of SRAM Cell. Since the technology used is 90 nm. Hence the DC supply voltage reduced to 1.0 volts

5. CONCLUSION

The 90 nm and 180 nm SRAM Cell is device designed & simulated by using Visual TCAD software and read and write operation of the SRAM is studied. Scaling of devices leads to reduction in the supply voltage and hence power decreases but stability of the cell decreases. From the simulation result, the effect of scaling is studied and optimum value of V_t at 90nm technology is 0.2568 V is obtained. The value is in accordance with ITRS guidelines. Further SRAM device structure is designed using GENIUS TOOL.

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