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Acquisition of High Frame Rate Ultrasound Data through Ethernet for Telemedicine Applications

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Abstract: **Diagnosis of cancer involves assessment of elasticity by which the parameters such as density and velocity are evaluated. The velocity of the induced shear waves orthogonal to the ultrasound wave propagation is used to determine the stiffness of tissues for distinguishing between malignant and benign in transient elastography. For computing the speed of shear wave propagation an ultrafast scanner is required to gather the huge amount of data for interpretation in receiver engine. An algorithm is used which reduces the data sent to processing engine within handling range of the laptop. Information from scanner is ported for processing through standard Ethernet interface. Data from piezoelectric crystals are stored in FPGA databanks and converted into Packets. The layered model of User Datagram Protocol, Internet Protocol and Ethernet frame contains data and overheads bytes. The Data is transferred to laptop through Gigabit Ethernet Media Access Control and Gigabit physical layer devices. The packets received in laptop are observed using standard software tools. The raw data can be analyzed remotely by experts in laptop which involves parallel receive beam forming, image display and velocity detection using Graphical User Interface. Standard Ethernet hardware interface enables data processing in laptop which reduces the overall cost and size of the hardware enabling the methodology to be used for telemedicine applications in rural areas.**

Keywords - Transient elastography, malignant, benign, Parallel receive beam forming, Ethernet frame overheads, Media Access Control, Internet Protocol Packets, Field Programmable Gate Array, databank, User Datagram Protocol, Graphical User Interface , telemedicine.

1. INTRODUCTION

The tumor in the body can be imaged and detected non-invasively in B mode scanning using medical ultrasonography.

1.1. Medical Diagnosis of Cancer

A confirmative invasive test is done with biopsy in many suspicious cases even though detection and diagnosis is carried out using ultrasonography. Usually a benign tumor appears as a well defined margin as shown in Figure-1 on ultrasonography.

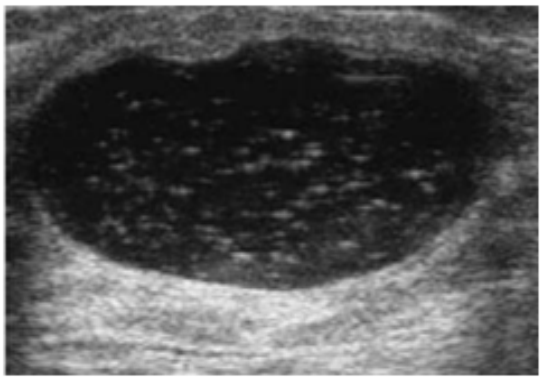

Figure-1: Benign tumor

As the malignant tumors are metastasis in nature, they can be classified into various BIRADS scores. Usually a malignant appears to be in an irregular shape as shown in Figure-2.

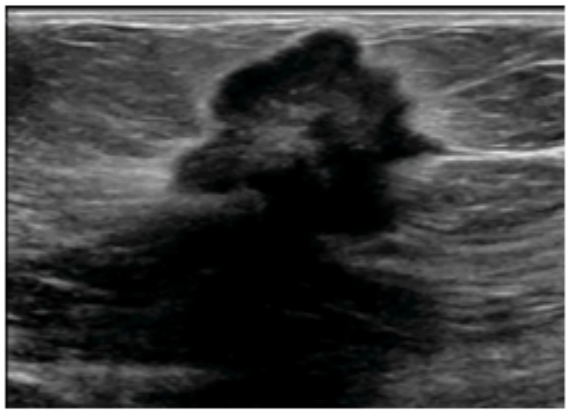

Figure-2: Malignant cancer

Sometimes pitfalls are found in the diagnosis of cancer. Figure-3 is a biopsy proven malignant tumor. But in ultrasonography, it appears to be a benign mass as it has a well defined margin. It is an infiltrating ductal carcinoma mimicking a benign mass.

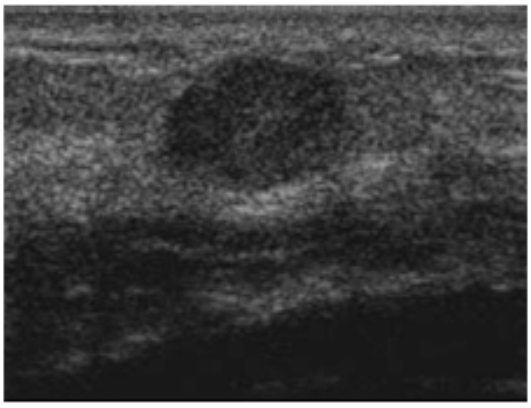

Figure-3: Malignant mimicking benign

The ultrasonography image of the suspicious tumor in Figure-4 appears as a malignant tumor as it is having an irregular shape and was classified in BIRADS-5 score. But actually biopsy proved this to be benign sclerosing adenosis.

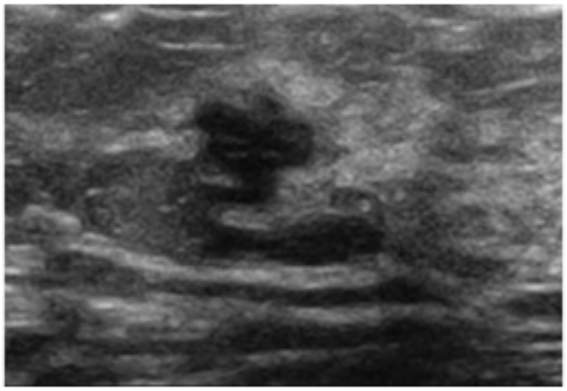

Figure-4: Benign mimicking malignant

Biopsy confirms the nature of the tumor whether malignant or benign. But, biopsy is a painful invasive procedure. Hence for conformation, an alternative method of tissue stiffness measurement using elastography is opted.

1.2. Elastography Measurements

The elasticity can be measured using two formulae one by using the ratio of stress and strain which is static elastography [1]. The other method known as Transient Elastography uses the calculated velocity of the generated shearwaves. The elasticity is proportional to the square of velocity.

The tumor is diagnosed for malignant or benign based on their tissue characteristics as malignant tissues are more stiff than the benign. Here, low frequency shear waves are induced by vibration force which propagates at a low speed of a few m/s. It produces two types of waves in the medium i.e. a compression or P wave as well as a Shear or S wave. The P waves travel in the direction of the ultrasound wave. The S waves travel orthogonal to the ultrasound waves. The frame rate of the detection machine is higher than 1000 frames/s for measuring the propagation [2]. The movement of the shear waves is monitored using an ultrafast scanner at high frame rates. The velocity of shearwaves is measured by calculating the arrival time between frames. The elasticity of the material is quantitatively measured in Kilo Pascal (kPa).

1.3. Requirement of Ethernet Interface

In a portable transient elastography machine the data and image processing is done in laptop. Standard interfaces such as USB or Ethernet is used between the machine and laptop. Even though Laptops have Gigabit Ethernet interface, they can receive continuous data without loss of packets only for speeds around 50Mbps. Hence the scanned data sent from the ultrasound scanner to the laptop is of the order of around 50Mbps for reasonable processing and display in the laptop. The raw data in standard formats or the converted video data are also possible to be sent to a remote location for telemedicine applications. Thus it requires reduced throughputs. Hence peak throughput and TCP window sizes are required to be determined for optimum use of the resources [3].

2. MATERIALS & METHODS

2.1. General Working Procedure of Ultrasound

A general block schematic is given in Figure-5.

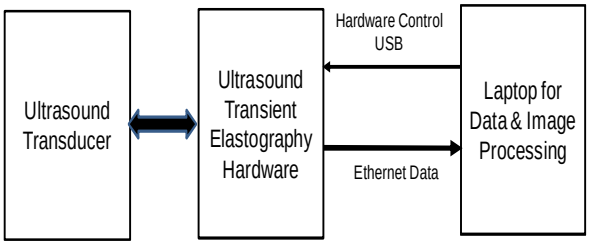

Figure-5: Generalized Block schematic

The Tx FPGA generates the Transmit pulses between 3 to 8MHz. The Pulse Repetitive Frequency (PRF) is common for all the channels. The High Voltage Pulser has 8 Channels and consists of logic interfaces. The HV Pulser amplifies the digital pulses generated by the FPGA for exciting the Piezo electric crystals located in the Ultrasound transducer probe. The 8 channel receiver consists of Low Noise Amplifier (LNA), Variable Gain Amplifier (VGA), Anti-Aliasing Filter (AAF), and ADC. In the receiver section the LNA is used to amplify the low level receive signals that are received from the piezoelectric crystals. The Time Gain Compensation (TGC) using VGA compensates for the receiving time delay. The Anti-Aliasing Filter (AAF) filters the signal and Analog

to Digital Conversion (ADC) does the Analog to Digital conversion. These functions of ultrasound are implemented in the receiver chips in [5].

The internal RAM of the FPGA acts as the temporary storage of the scanned data. The data received from the LNA is stored in one bank of the FPGA RAM. Simultaneously data from the second data bank is packetized and sent to the Gigabit Ethernet MAC device.

Gigabit Ethernet controller supports full duplex operation with 1000Mbps data Rate. It does the Ethernet framing of the data. Physical Layer (PHY) device carries out the Physical layer level translations and conversions to Gigabit Ethernet speeds over copper interface.

The data processing and image processing is carried out in the MATLAB based GUI. The device configurations are controlled from the GUI through a microcontroller in the Ultrasound board.

2.2. Efficient algorithms for reducing the output data rates

An ultrasound machine working on the principle of transient elastography operates at frame rates of over 1000 frames per second. The Ethernet data calculations in such cases are given in Table-1 below.

Table-1: Ethernet Data Rate Calculations

Ultrasound Frequency	Sampling Frequency	Bits per sample	Number of Channels	Data Rate
8MHz	60MSPS	12	64	46Gbps
8MHz	40MSPS	8	64	20Gbps
8MHz	24MSPS	8	64	12Gbps
6MHz	24MSPS	8	32	6Gbps

Receiving this huge volume of data and processing is a challenge for portable low cost ultrasound machines. The Laptops have 10/100/1000 Mbps Ethernet interface. It is easy to transfer and view the images immediately on a laptop at a distant location using Gigabit Ethernet interface [4]. An interface at wire rates while working at 1000Mbps can receive a maximum data rate of around 600 to 700Mbps while the balance data is wasted as Ethernet frame and IP overheads.

The Laptop interface never works at wire rates. They are designed for burst type of Ethernet data traffic. Hence for continuous data, these interfaces work less than 2% of their maximum capacity. Hence the typical data rates need to be around 50Mbps for receiving through Ethernet interfaces of Laptops without data loss. Such a machine uses data compression techniques such as averaging and peak detection for reducing the per channel data rates. Moreover, they use efficient algorithms to reduce the data rates to the practical limits without sacrificing on the frame rates. The Ethernet data throughputs required in the last case of Table-1 because of the above techniques is given below.

Table-2: Throughput due to compression

Method	Throughput Reduction	Throughput
Peak detection of consecutive 8 samples	8	750Mbps
Selected window transmission	16	47 Mbps

This reduction of data throughput without sacrificing the frame rate requirements for Transient Elastography enables the data to be captured through Ethernet Interfaces for processing.

2.3. Data framing requirements:

The data is required to be in frames as per the Ethernet framing standards for the data link layer, IP framing standards for the IP layer and UDP framing standards for the Transport layer. The overall framing architecture and individual framing details are given in Figure-6.

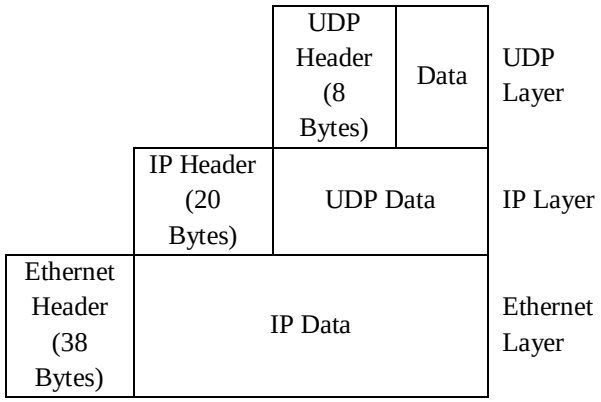

Figure-6: Overall framing architecture

The Ethernet framing requirements is as per IEEE 802.3 standards in the Ethernet layer architecture. The interface logic is embedded in the Field Programmable Gate Array (FPGA).The user logic is also [6] embedded in the same FPGA. Ethernet Frame with IP/UDP Packet is created by the FPGA.

IP layer Packet architecture, byte requirements is as per RFC791 standard. The source and the destination IP address are assigned through the GUI interface.

The UDP datagram architecture is as per RFC768. The UDP overheads has the UDP Source/destination port 104 (68 Hex) which corresponds to Digital Imaging and Communication in Medicine is used as the standard port. For achieving high data throughput, the UDP/IP protocol having Jumbo frames is employed. In reference [7], a minimal UDP/IP stack realized in FPGA providing hard real time transmission is designed in Ethernet frames for different purposes.

The interface bus between the FPGA and the Gigabit Ethernet MAC device is 32 bit wide. 3 clocks i.e. 2 clocks at the start are used for start of data and one clock in the end of frame is used for end of frame communication from FPGA to the Gigabit Ethernet MAC.

2.4. Choosing the FPGA

For logic emulation systems the Field Programmable Gate Array (FPGA) provides faster computation as compared to software simulation. The logic designs are customized for high performance in different types of applications. In multimode system, the FPGA yield significant hardware savings and provides generic hardware in [8]. In order to meet the above requirements, the Xilinx FPGA with the following specifications is chosen. The FPGA has 172 input/output (I/O Pins), 216K Blocks of RAM, LVDS (Low Voltage Differential Signaling) is used for interfacing with High Voltage Pulser and Receiver chips. The speed of the IO Bus is 622Mbps, with EEPROM having Master-Slave/JTAG Programming Headers.

2.5. FPGA Receive System Architecture

The FPGA receive system architecture is given in Figure-7. The Analog to Digital conversion function in the receiver section is interfaced with Field Programmable Gate Arrays in [10]. The FPGA design can be sub-divided into four sections i.e. the clock generation, channel data receiver, data storage and packet formation sections. The clock generation section generates all the required clocks from a crystal oscillator source clock. The data from the receiver is in the low voltage differential signaling (LVDS) format. The channel data receiver contains the LVDS receiver, serial to parallel converter which converts the data to byte serial format and the peak detector.

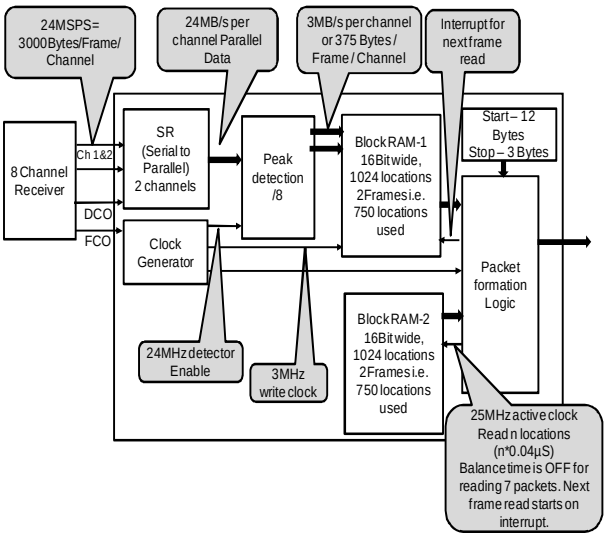

Figure-7: Receive FPGA logical block schematic

The data storage section stores the data in two data banks. The packet formation logic further converts the data into packets which is explained in flow chart in Figure-8. The pipelined architecture of the Field programmable gate array and the distributed Random Access Memory for high I/O resources of an image classifier implementing object classification stages in object detection system is discussed in [11].

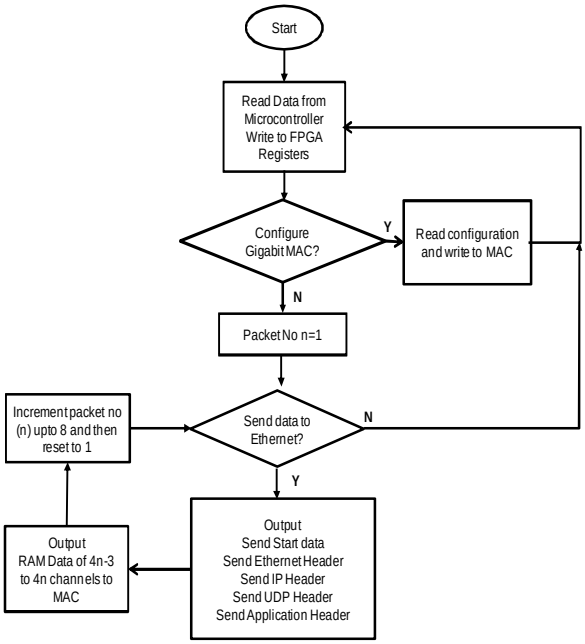

Figure-8: Receive FPGA software algorithm flow chart

The microcontroller through the USB interface controls the start and stop of the operation. The FPGA reads the data from the microcontroller and writes to FPGA registers. The FPGA configures the Gigabit MAC control registers. The FPGA

forms the packets in the sequence of Start data, Ethernet Headers, IP Headers, UDP Headers, Application Header and RAM data from the correct RAM position.

3. IMPLEMENTATION & SIMULATION

3.1. Storing the receive data in the FPGA RAM using two data banks

The LNA supplies two clocks FCO and DCO for synchronizing and reading the data by the FPGA LVDS Receiver. Various clocks required for receiving and processing of the data are generated in the FPGA. The receive data is converted into serial to parallel stream and stored in the FPGA Block RAM. Two blocks RAM's of the FPGA are used for writing the alternate frame of data. Likewise all the 32 channels of receive data are written into the databanks.

3.2. Storing Overhead data in FPGA Registers

The overhead data for the Ethernet Frame, IP Packet and UDP datagram are stored in the FPGA Registers. Some of these data values are fixed values where as some of the values like source, destination IP addresses etc are assigned by the Microcontroller. The Microcontroller in turn is programmed from the MATLAB GUI through the USB interface.

3.3. Reading data from the databanks

In the experimental setup described in this paper, the data is divided into multiple windows. i.e., each window comprises of 16 bytes per channel. During one write cycle to the FPGA, only one window of 16 x 32 bytes is transferred to the laptop and balance data is discarded. A multi frame consists of 256 such sub frames. Once one multi frame is read, it moves on to read the next window and so on. This also ensures that high frame rate is retained so that the measurement of frame to frame displacement and hence the transient wave velocity is not affected.

3.4. Packet formation of the data

Ethernet communication in FPGA uses Reduced Media Independent Interface (RMII) a standard to reduce the number of signals required to connect a PHY to a MAC in physical layer [12]. The RMII four channels are put in one Ethernet frame.

Counters are used for sending the data sequentially in the order of start bits, Ethernet header, IP header, UDP header, Application header, Data from the block RAM, Ethernet end of frame and stop bits. During the Start send MAC period, Start byte for the Gigabit MAC device is send. During the Start Send Overheads period, all Ethernet, IP and UDP overheads are read from the registers and send. During the Start Send data period, the data from the FPGA RAM is send using the read clock. During the Stop send data, Ethernet Stop bits and Stop byte for the Gigabit MAC are sent.

4. RESULTS

Data or the packets captured are shown in the figure 9.

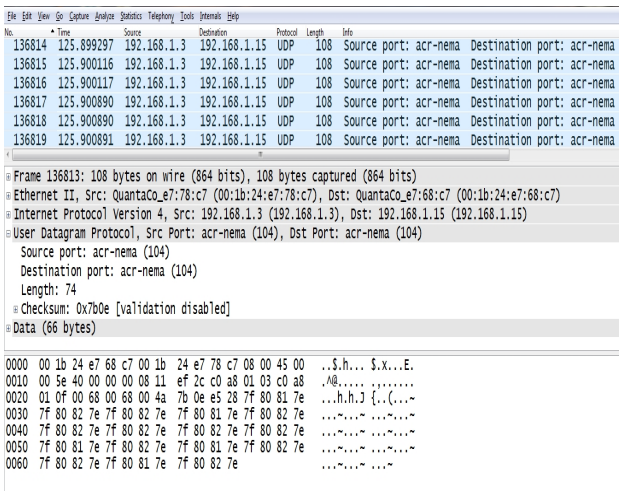

Figure-9: A snapshot of the packets captured

The UDP datagram port 104 (00 68) Hex corresponds to ACR-NEMA (American College of Radiology (ACR) and the National Electrical Manufacturers Association (NEMA)) which corresponds to the DICOM (Digital Imaging and Communications in Medicine) standard is seen highlighted. The packet rate or the frame from the above figure is seen around 8000 packets per second. The size of the frame has 108 bytes with the packet size of 94 bytes and UDP size of 74 bytes (00 5e) Hexadecimal ,with data size of 66 bytes (2 bytes for overhead and 64 bytes for data)as seen from the results. Further, the displacement of the propagating shear wave is measured as a function of time and space [13] using MATLAB based algorithms.

5. CONCLUSION AND DISCUSSION

For observing the shearwave propagation and to compute the shear modulus, an ultrafast scanner is required which works at frame rates more than 1000 fps. The developed prototype of the ultrasound machines was able to collect huge amount of scanner data and process the same in the processing engine. The algorithms reduce the amount of data sent to the processing engine. Such data from the scanner could be ported to Laptops for processing through standard interfaces such as Ethernet. The data collected from the different channels is converted into packets in a standard and intelligent way and sent over standard Ethernet interfaces in a seamless way for processing at the Laptop.

The processing in the Laptop is done using MATLAB based GUI. This processing involves receiving the packet data, conversion of the packets into data matrix, inverse mapping for moving window algorithm, parallel receive beam forming of the received data and motion detection using inter frame displacement measurements.

The relocate of healthcare information of Telematics applications between institutions is very off the record. Hence there should be a protected method of transfer of information. Such a methodology and Framework is of importance in patient's treatment [14]. This is easily achieved using Ethernet protocols. Minimization of latencies introduced by the network is achieved by the employment of a User Datagram Protocol (UDP) channel. The performance of ACR/NEMA 300, a digital imaging and communication standard for medical picture archiving and communication systems (PACS), proposed by the American College of Radiologists (ACR) and the National Electrical Manufacturers Association (NEMA) in terms of image delay, using simulated images, please see [15].

This makes the transient Elastography technology viable and cost effective for use in telemedicine applications.

6. ACKNOWLEDGEMENTS

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