Journal of Basic and Applied Engineering Research
Print ISSN: 2350-0077; Online ISSN: 2350-0255; Volume 1, Number 10; October, 2014 pp. 4-19

http://www.krishisanskriti.org/jbaer.html

Review of Flip-Flop

Divya Aggarwal

Student, Department of Physics and Astro-Physics, University of Delhi, New Delhi

Abstract: **The world is growing at an extra fast speed and so is technology. Today small devices with maximum efficiency are in demand and so came the flip flops. In electronics, they are used as data storage elements which can store state. They can be either simple or clocked; here we will discuss all of them such as S-R Flip Flop, J-K Flip Flop, D-Flip Flop. There are Positive edges triggered as well as Negative edge triggered Flip Flops. They can also be connected together to form a master slave such that race around condition can be avoided .All of these topics will be discussed in detail in the paper**

Flip Flop

1. INTRODUCTION

A **sequential circuit** consists of a *feedback path*, and employs some *memory elements.*

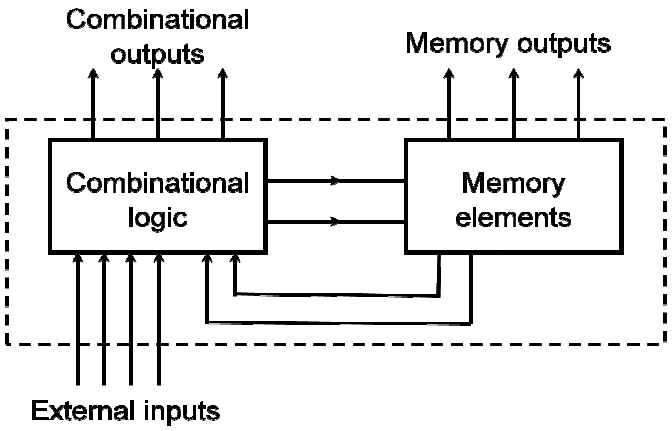

Fig. 1: sequential circuit

Sequential circuit = Combinational logic + Memory Elements

There are two types of sequential circuits:

a. *synchronous*: outputs change only at specific time

b. *asynchronous*: outputs change at any time

***Multivibrator*:** a class of sequential circuits. They can be:

- *bistable* (2 stable states)
- *monostable* or *one-shot* (1 stable state)
- *astable* (no stable state)

Bistable logic devices: *latches* and *flip-flops*.

Latches and flip-flops differ in the method used for changing their state.

Flip-flop also called as latch is a circuit or a bi-stable multivibrator that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic and is used in computers, communications, counting of pulses, synchronizing variably-timed input signals and many other types of systems.

When used in a finite-state machine, the output and next state depend on its current input and also on its current state (and hence, previous inputs). Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered A latch is level-sensitive, whereas a flip-flop is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop's output only changes on a single type (positive going or negative going) of clock edge.The difference between a latch and a flip-flop is that a latch is asynchronous, and the outputs can change as soon as the inputs do (or at least after a small propagation delay). A flip-flop, on the other hand, is *edge-triggered* and only changes state when a control signal goes from high to low or low to high.

Memory element:

a device which can remember value indefinitely, or change value on command from its inputs.

Characteristic table:

$Q(t)$: current state

$Q(t+1)$ or Q^+: next state

Clock is usually a square wave.

Command (at time *t*)	*Q(t)*	*Q(t+1)*
Set	X	1
Reset	X	0
Memorise / No Change	0	0
	1	1

Fig. 2: characterstic table

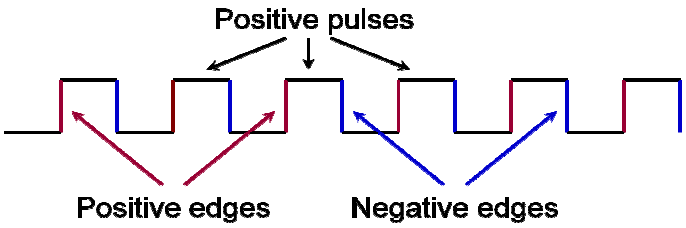

Fig. 3: Clock output

Two types of triggering/activation:

a. pulse-triggered
b. edge-triggered

in Pulse-triggered latches are ON = 1, OFF = 0 whereas in Edge-triggered flip-flops are:

a. positive edge-triggered (ON = from 0 to 1; OFF = other time)
b. negative edge-triggered (ON = from 1 to 0; OFF = other time)

There are several different types of flip-flop each with its own uses. The four main types of flip-flop are :

SR
JK
D

SR Flip Flop

a) NOR gate Latch

The design of such a flip flop includes two inputs, called the SET [S] and RESET [R]. There are also two outputs, Q and Q'. when Q is high, the latch is in SET state whereas when Q is low, the latch is in RESET state. For active HIGH input S-R latch also n\known as NOR gate latch
R=HIGH & S=LOW==RESET state
S=HIGH & R=LOW==SET state
BOTH INPUTS low ==no change

BOTH INPUT HIGH== Q and Q' both LOW (invalid) and *Q'*.

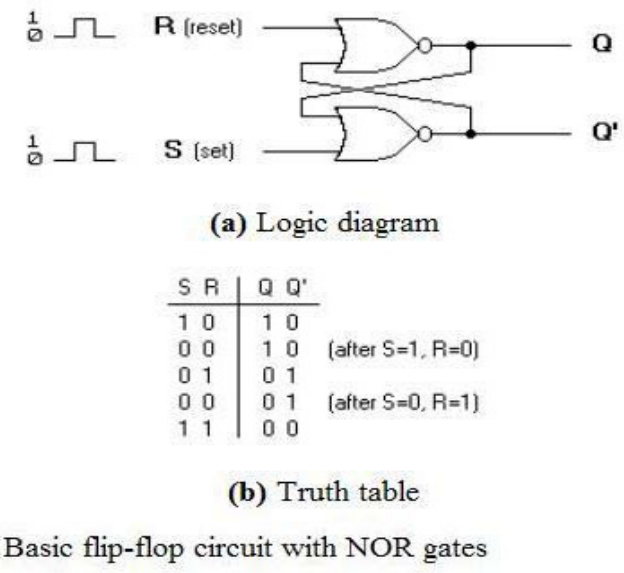

Fig. 4: flip flop with NOR gate

b. NAND gate Latch

For *active-LOW input* S'-R' latch (also known as NAND gate latch),

- *R'*=LOW (and *S'*=HIGH) a RESET state ;
- *S'*=LOW (and *R'*=HIGH) a SET state
- both inputs HIGH a no change
- both inputs LOW a *Q* and *Q'* both HIGH (invalid)!

Drawback of S-R latch: invalid condition exists and must be avoided.

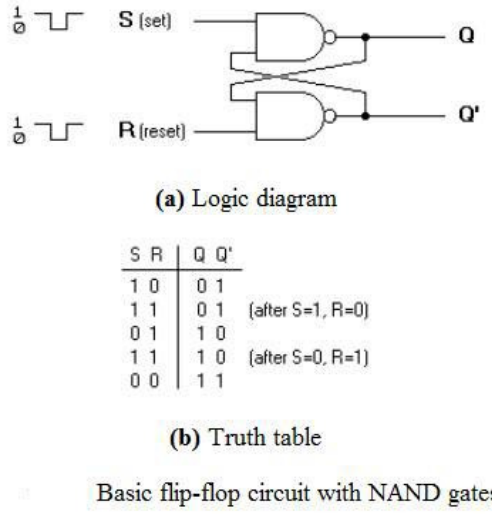

Fig. 5: flip flop with NAND gate

JK Flip Flop

In J-K flip-flop Q and Q' are fed back to the pulse-steering NAND gates. There is no invalid state and it Includes a *toggle* state.

- *J*=HIGH (and *K*=LOW) a SET state
- *K*=HIGH (and *J*=LOW) a RESET state
- both inputs LOW a no change
- both inputs HIGH a toggle

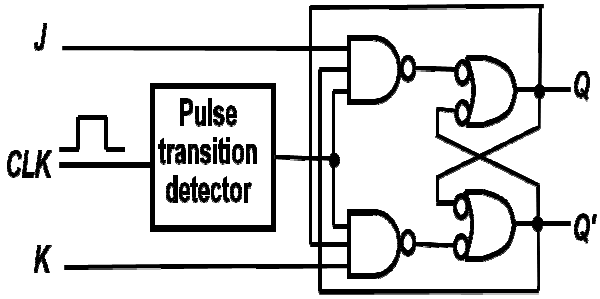

Fig. 6: J-K Flip flop

J	K	CLK	Q(t+1)	Comments
0	0	↑	Q(t)	No change
0	1	↑	0	Reset
1	0	↑	1	Set
1	1	↑	Q(t)'	Toggle

Fig. 7: truth table

Q	J	K	Q (t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Fig. 8: truth table

D-Flip Flop

- D flip-flop is a single input *D* (data) where
- *D*=HIGH a SET state
- *D*=LOW a RESET state

Q follows *D* at the clock edge.

We can convert S-R flip-flop into a D flip-flop by adding an inverter. A positive edge-triggered D flip-flop formed with an S-R flip-flop.

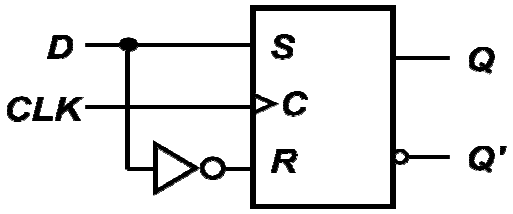

Fig. 9: D Flip Flop

D	CLK	Q(t+1)	Comments
1	↑	1	Set
0	↑	0	Reset

Fig. 10: truth table

The Application of D-Flip Flop is Parallel data transfer. it is used to transfer logic-circuit outputs X, Y, Z to flip-flops Q_1, Q_2 and Q_3 for storage.

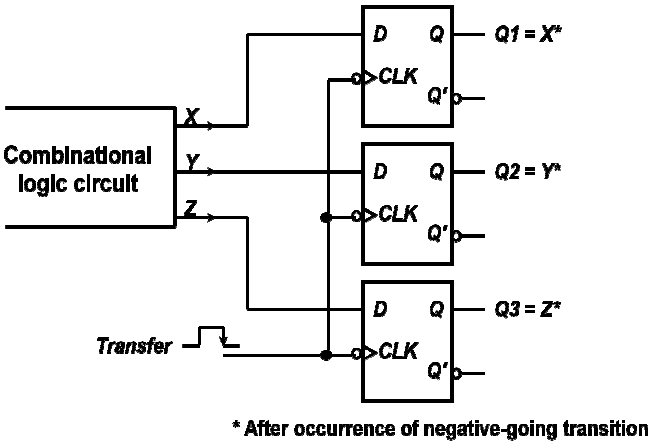

Fig. 11: Parallel data transfer

Edge Triggered Flip Flop

Edge triggered flip-flop changes only when the clock C changes. An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input. The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. On the other hand, the direct set (SET) and clear (CLR) inputs are called

asynchronous inputs, as they are inputs that affect the state of the flip-flop independent of the clock.

Few truth tables of S-R, J-K and D flip flop are:

Inputs		Outputs		
D	C	Q	Q'	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

Fig. 12: S-R Flip Flop

Inputs			Outputs		
J	K	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	Q'	Q	Toggle

Fig. 13: J-K Flip Flop

Inputs			Outputs		
S	R	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

Fig.14: D Flip Flop

MASTER-SLAVE

We can use a clock to synchronize our latches with the ALU.The clock signal is connected to the latch control input C.The clock controls the latches. When it becomes 1, the latches will be enabled for writing.

The clock period must be set appropriately for the ALU. It should not be too short. Otherwise, the latches will start writing before the ALU operation has finished. It should not be too long either. Otherwise, the circuit will be slower than necessary.

The **Master-Slave Flip-Flop** is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the "Master" flip flop being connected to the two inputs of the "Slave" flip flop. If the circuit is a master-slave D flip-flop then it takes only a single input, the D (data) input. The master-slave configuration has the advantage of being edge-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output.

The circuit consists of two D flip-flops connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state. A master-slave flip-flop is normally constructed from two flip-flops: one is the Master flip-flop and the other is the Slave. In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted CP is given to the slave flip-flop. For example, if the CP=0 for a master flip-flop, then the output of the inverter is 1, and this value is assigned to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop.

A master-slave flip flop can be constructed using any type of flip-flop which forms a combination with a clocked RS flip-flop, and with an inverter as slave circuit.

When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state.

The result is that output can only change state when the clock makes a transition from high to low.

For example: J-K Flip flop

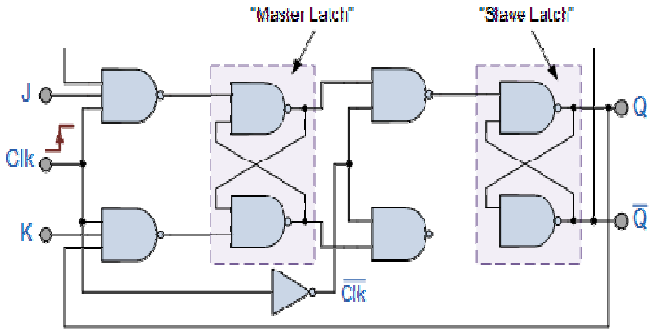

Fig. 15: J-K Flip Flop master slave

During the positive edge of the flip-flop, the information from external inputs J and K is passed through to the master flip-flop. It is held there until the negative edge transition of the flip-flop occurs. Then the information is passed to the slave, clocked RS flip-flop, and the output is observed. Usually the clock pulse is 0 at start, so the values of J and K will not affect the state of the system, and the master flip-flop is isolated. But the output of gate 9 is 1, hence the slave flip-flop provides the output Q=Y and Q'=Y'. When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.

Current digital systems make heavy use of master-slave flip-flops. The output of some master-slave flip-flops is given as an input to the other master-slave flip-flops. If the clock pulse inputs to all master-slave flip-flops are synchronized then at the beginning of each clock pulse, some of the master elements changes state. But the output remains in the previous state without any change (because slave is isolated and disabled). Again when CP returns to 0, the output changes sate and the master flip-flops are disabled. So the new state of output does not have any effect on the master input until CP=1. Therefore both the state of the system and the input elements can be changed simultaneously with a single clock pulse. So the binary content of one flip-flop can be transferred to second and the content of second can be transferred to first simultaneously during the same clock pulse. . In other words, the **Master-Slave JK Flip flop** is a "Synchronous" device as it only passes data with the timing of the clock signal

The master-slave flip-flops are widely used in MEMORY REGISTERS.

REFERENCES

[1] http://en.wikipedia.org/wiki/Flip-flop_(electronics)
[2] http://en.wikibooks.org/wiki/Digital_Circuits/Flip-Flops
[3] http://www.circuitstoday.com/flip-flops
[4] http://isweb.redwoods.edu/INSTRUCT/CalderwoodD/diglogic/srflip.htm
[5] http://www.circuitstoday.com/flip-flops cs1104-11 presentation
[6] http://osp.mans.edu.eg/cs212/FF_Edge_Triggered.htm
[7] http://www.falstad.com/circuit/e-masterslaveff.html
[8] http://www.electronics-tutorials.ws/sequential/seq_2.html
[9] http://www.electronics-tutorials.ws/sequential/seq_2.html