A Quantum Mechanical Mobility Analysis of Surrounding Gate Transistor (SGT)

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ABSTRACT

As transistor is scaled down, beyond the certain limit, some parameter cannot be scaled down such as gate oxide thickness (t_{ox}) and threshold voltage (V_{th}). Due to this, Leakage and Delay are increased which slow down the performance of transistor. And Short Channel Effect (SCE) become more severe below 20 nm gate length and Multigate transistor structure such as double gate, triple gate and surrounding gate transistor are needed to meet performance requirement. Surrounding gate transistor (SGT), due to its better electrostatics control on channel potential, can address this limitation. Surrounding gate transistor (SGT) is a transistor in which gate material surrounds the channel region on all sides. This multi-gate transistor reduces the coupling between threshold voltage and leakage current. But this advantage is overshadowed by mobility degradation. The quantum mechanical effects become dominant factor in surrounding gate transistor. These quantum mechanical effect and mobility degradation are studied and analyzed. The impact of quantum mechanical effect on device characteristics such as threshold voltage, drain current, electron density and mobility are explored. The effect of device dimension (Gate oxide thickness (t_{ox}), Gate Length (L), Thickness of silicon tube (t_{si}) on electron mobility is also explored. It was found that threshold voltage is increased by some milivolt. Due to this drain current is decreased. It is also found that there is a shifting of peak electron density away from Si-Si_{O2} interface. Impact of quantum mechanical effect on electron mobility is also found. Due to quantum mechanical effect, effective mobility is decreased. The impacts of device parameter of surrounding gate transistor are also observed. If thickness of oxide (t_{ox}), thickness of silicon tube (t_{si}) and gate length (L) is decreased, mobility is also decreased. It is also found that the effect of t_{ox} on electron mobility is more at interface than centre.

Keywords— Scaling Theory, Short Channel Effect, Mobility, Quantum Mechanical (QM) Effect, Surrounding Gate Transistor, Multi-gate device

1. INTRODUCTION

As device scaling continues for the 21st century, it turns out that the historical growth, doubled circuit density and increased performance by about 40% every technology generation, followed by MooresLaw; cannot be maintained only by the conventional scaling theory. Increasing leakage

current does not allow further reduction of threshold voltage, which in turn impedes further supply voltage scaling for the historical speed improvement. Accordingly, generated higher electric fields inside of the transistor worsen device reliability and increase leakage currents. Moreover, the required high channel doping causes significant challenges such as mobility degradation, increased band-to-band tunneling (BTBT), gate-induced drain leakage (GIDL) and random dopants induced threshold voltage fluctuations. Due to those ever increasing short channel effects (SCEs), there have been several strategies introduced for CMOS device to extend Moore's law. A few examples of those are; increasing electrostatic control over the channel by means of the continuous equivalent oxide thickness (EOT) scaling with high-k/metal gate stack, multi-gate structures for higher drive current at the constant over-drive voltage, improving carrier mobility by adopting high mobility channel materials, and strain engineering and reducing parasitic.

In addition, various researches have been actively carried out in device domain to find an alternative device to continue to sustain Moore's Law. Among these efforts, various kinds of alternative memory and logic devices (beyond CMOS devices) have been proposed. These nano devices take advantages of the quantum mechanical phenomena and ballistic transport characteristics under low supply voltage and consume low power. Furthermore, due to their extremely small sizes, those devices are expected to be used for ultra-high density integrated electronic components having billions of devices in a single chip. The electrostatics gets improved in multiple-gate structure as the gate influences the channel potential from more than one side. The Gate-All-Around structure is the most resistant to short channel effects among all the emerging nano device structure. As the channel length reaches to nanoscale, quantum mechanical effects are manifest. In this work, the quantum mechanical effects on the electron effective mobility of the SG nMOSFETs in nanosize, and how the effects influence the transistor's performance.

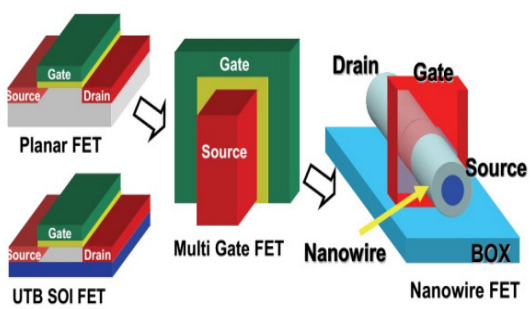

Figure 1: Transition of the device structure for enhancement of electrostatic controllability of the gate electrode on the channel (source: internet)

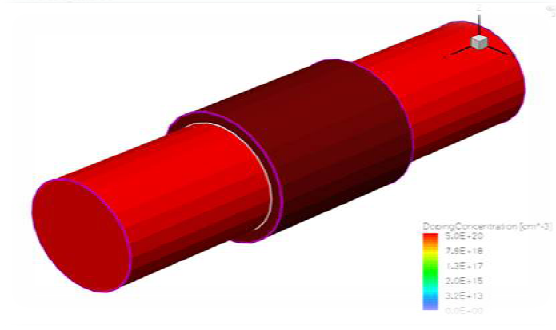

Figure 2: Gate-All-Around

2. QUANTUM MECHANICAL EFFECT IN NANO-SCALE DEVICE

Quantum Mechanical (QM) Effect arises when a large electric field at the interface of Si-SiO_2 leads to Quantum Mechanical effect. Due to high electric field, there is a formation of a potential well, which confines charge carriers to a region close to the Si-SiO_2 interface. Carrier are free to move parallel to the interface, but are tightly confined in a short distance from the Si-SiO2 interface. There are so many quantum mechanical effects. But some are Quantum Mechanical Confinement and Quantum Mechanical Tunneling. This Confinement leads to quantized energy levels thus the conduction band and valance bands are split into sub bands. Quantum confinements take place when the quantum well thickness becomes comparable at the de-Broglie wavelength of the carriers [10]. Quantum well which confine the charge carriers (electrons / holes) in one dimension and allow free prorogation in other two dimensions [1]. The thickness and/or width of multi-gate FETs is reaching values that are less than nano-meters. Under these conditions the electrons in the two-Dimensional Electron Gas (2DEG) if we consider a double-gate device or a one-Dimensional Electron Gas (1DEG) if we consider a triple or quadruple-gate MOSFET. Consider a double-gate device made in a thin silicon film. The film thickness being t_{si}, electrons are free to move in the x and z direction, but they are confined in the y direction. In a thin and narrow triple-gate or quadruple-gate device electrons are free to move in the x direction only, and are confined in the y and z directions. This results in the formation of energy sub bands and in electron distributions in the silicon film that can be significantly different from what is predicted by classical theory. In particular, inversion layers need not to be localized at the surface of the silicon film, but can instead be found in the depth of the film, giving rise to volume inversion. The confinement of electrons is also at the origin of new and previously unexpected mobility and threshold voltage behavior. In classical device simulations, using drift-diffusion approximation the peak of the electron concentration in channel of a turned on a n-channel MOSFET is calculated to be directly at the interface. This is not correct as the number of allowed states is drastically reduced close to the interface and therefore the peak of the carrier concentration lies several angstroms away from the interface. So, classical theory will not be sufficient to explain the Quantum Mechanical effect [1].To correctly predict volume inversion one needs to solve both the Schrödinger and the Poisson equation in a self-consistent manner.

The quantization effect is more complicated in Surrounding-Gate (SG) Transistor than in bulk MOSFETs due to the extra structural confinement by the thin body. Due to Quantum Mechanical effects, Some parameter of device are affected which are Increased threshold voltage (V_{th}), Lower drain current (I_{ds}), Reduced inversion layer charge density, Modified carrier mobility, Increased effective band gap, Modified inversion charge profile, Modified surface potential, Increased effective oxide thickness(t_{ox}).

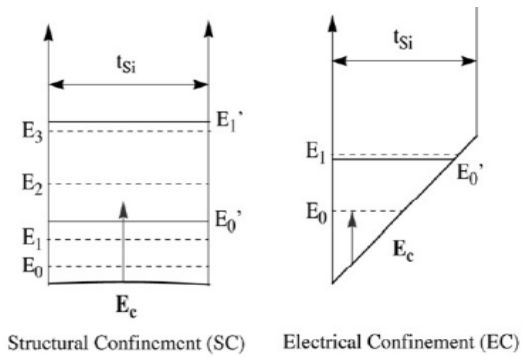

Figure 3: Structural Confinement and Electrical Confinement [1]

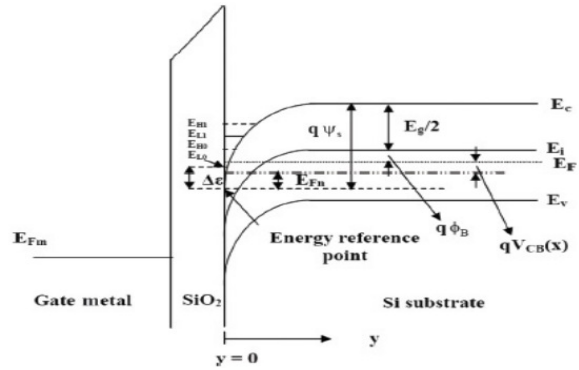

Figure 4: Energy band diagram of a metal/SiO_2/p-Si structure showing four lowest sub-bands [1]

As the device dimensions are scaled to the sub-100nm range, QM effects affect the device properties, Such as effective oxide thickness, inversion layer charge density and profile, threshold voltage, effective band gap, gate capacitance, mobility, surface potential, sub threshold characteristics, drain current and gate leakage current. Due to very small longitudinal dimension, confinement comes to picture in nano-scale bulk MOSFET [1]. Due to confinement, quantization takes place in conduction band. This leads to energy quantization in conduction band. Due to this, the lowest energy level of quantized conduction band is at little bit higher energy level [1] as shown in fig.3. As shown in fig.4, the peak electron density is shifted away some distance from Si-SiO_2 interface. And classical and quantum mechanical electron concentration distribution are different. At interface, Electron density is less due to quantum effect. At near of Si SiO2 interface, density of state is so less due to quantization of energy. Due to shifting of electron density away from Si-SiO_2, the effective thickness of oxide is increased. As a consequence of this, Drain Current (I_d) is decreased [1]. The electron concentration is maximum at some distance away from Si-SiO_2 interface [2]. This is called as Quantum-Mechanical Charge Distribution. This is obtained by solving the Schrödinger and poisson equation self-consistently and at centre of the GAA, Electron concentration is minimum due to presence of high electric field.

3. IMPLEMENTATION DETAILS AND EXPERIMENTAL RESULT

To make the device structure of Gate-All-Around, Parameter Description are Radius of the silicon(R) = 7.5 nm, Length of GAA (L) = 60 nm, Peak Phosphorous Doping Concentration (N_A) = 5e+20 1/cm^3, Gate oxide thickness (t_{ox}) = 1.5 nm, Work Function of Gate Electrode = 4.7 eV, Channel Length (L_g) = 20 nm, Length of source and Drain 20 nm, Channel is undoped. These parameters are default parameter. If any change is made in device parameter that will be mentioned with that. The figure 5 shows the I_d - V_g variation curve which is drawn at V_{ds}=0.5V. The bohm quantum model is calibrated with Schrodinger – Poisson model. Because S-P model is accurate

model and it has high accuracy but it take large amount of time to simulate the 3D device. There are two major drawback of S-P model (1) High computation time and (2) S-P model cannot calculate flow of charge. So, to avoid this, BQM model is used and after calibration with S-P model, BQM model gives accurate result like a S-P model. In calibration Quasi-static C-V (QSCV) curve is taken by S-P model. And the same QSCV curve is taken by BQM model for different-2 α and γ and are the two parameters whose value are changed for calibration so that QSCV cure for both will become same. There is a Formation of potential well because thickness of silicon (t_{si}) is in nano meter range which leads to high electric field. Due to this high electric field, potential well is formed. Quantum

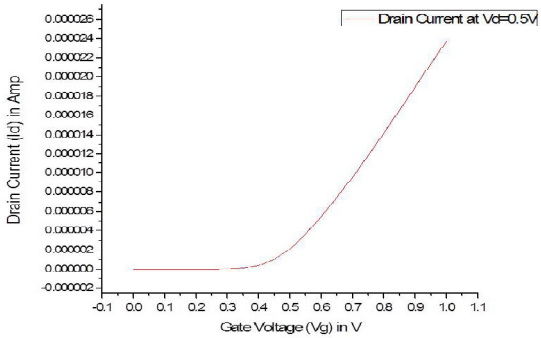

Figure 5: Drain Current at Drain Schrodinger- voltage of 0.5 V

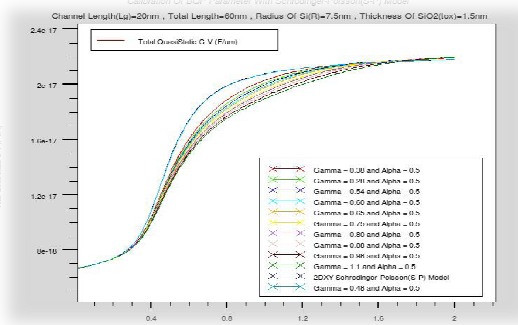

Figure 6: Calibration of with Poisson(S-P) Model

confinement effects come to picture when longitudinal length is scaled down. If lateral length is scaled down then quantum confinement will not appear.

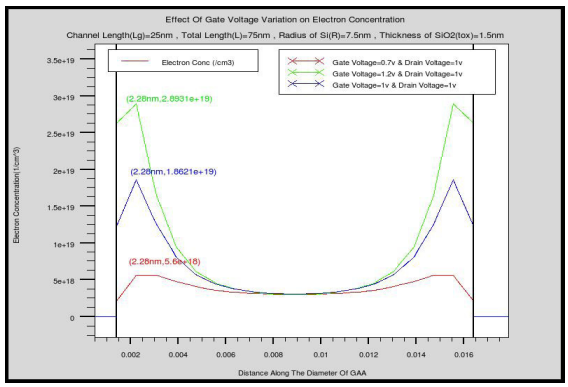

Figure 7: Variation of electron density along the diameter of GAA

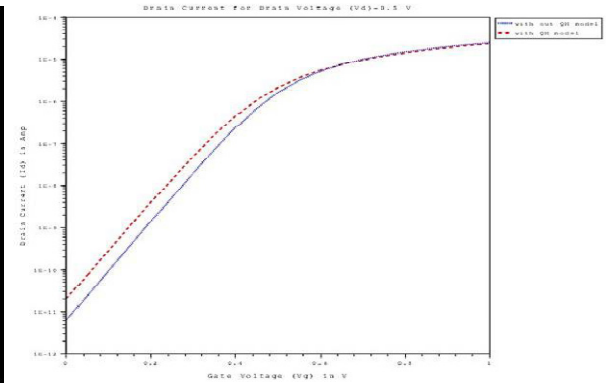

Figure 8: Threshold Voltage (V_{th}) Variation due to Quantum Mechanical (QM) effects

This figure 7 shows that there is Variation of electron density along the diameter of Gate-All-Around (GAA. It is shown in above figure 7 that the peak electron concentrations are shifted some distance away from the Si-SiO_2 interface. This is due to quantum mechanical effect. By increasing the gate voltage, shifted distance is changing but value of peak concentration is increasing and width of peak concentration is decreasing and channel is getting narrower. Due to this phenomenon, Effective gate oxide thickness (t_{ox}) is increased and effective gate oxide capacitance (C_{ox}) is decreased. The figure 8 shows that due to quantum mechanical effect, the threshold voltage of Gate-All-Around (GAA) is increased. It happens because effective gate oxide thickness (t_{ox}) is increased which decrease the gate oxide capacitance (C_{ox}). It is clearly shown in figure 11 that Drain current is decreased due to Quantum Mechanical (QM) effect. It happens because threshold voltage (V_{th}) is decreased. The relationship between V_{th} and I_d is given in equation 1.

$$I_d \alpha (V_{gs} - V_{th})^2 . \quad \text{…….. eq.} \qquad (1)$$

As gate voltage increases, Variation in drain current (I_d) increases. It has been clear that Drain current (I_d) with Quantum Mechanical (QM) model [9] is less than the Drain current (Id) without Quantum Mechanical (QM) model. This is due to increment in threshold voltage (V_{th}) leads to decrement in Drain Current (I_d). It is clear from figure 12 that the mobility is drastically reduced to nearly equal to zero at the surface. Because the Surface Roughness Scattering (SRS) is high at surface. It happens because of presence of high electric field at the surface of Gate-All-Around (GAA). The figure 14 shows the mobility variation inside the device which indicates the reduction in the value of mobility in the channel. If radius decreases then mobility will also decrease. The physics is that electric field is increased which give rise to scattering effect. If gate length increases then mobility would also increase because electric field is decreased which leads to less scattering. The effect of oxide thickness variation on mobility at center of Gate-All-Around is not more enough. But its effect at interface is more. If t_{ox} increases then mobility will increase because Gate field decreases.

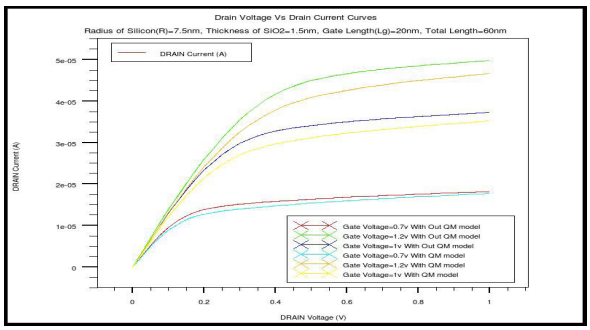

Figure 11: Drain Current (Id) Variation due along the to Quantum Mechanical (QM) effect

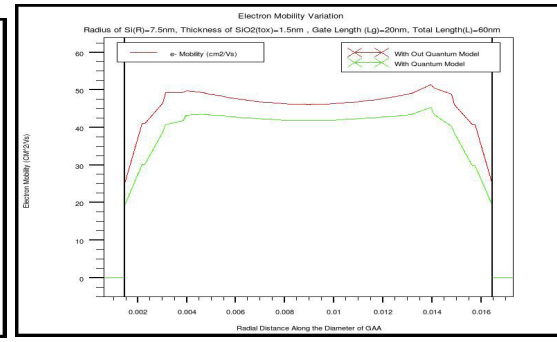

Figure 12: Electron Mobility Variation radial distance of Gate-All-Around (GAA)

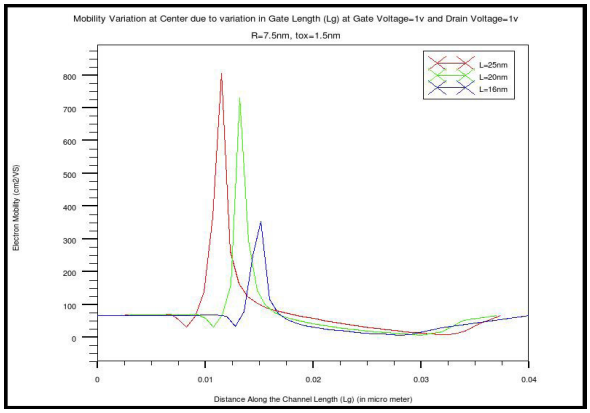

Figure 13: Mobility Variation at center due to variation in gate length of Gate- All-Around at Gate-All- Drain Voltage= 1v and Gate Voltage=1v.

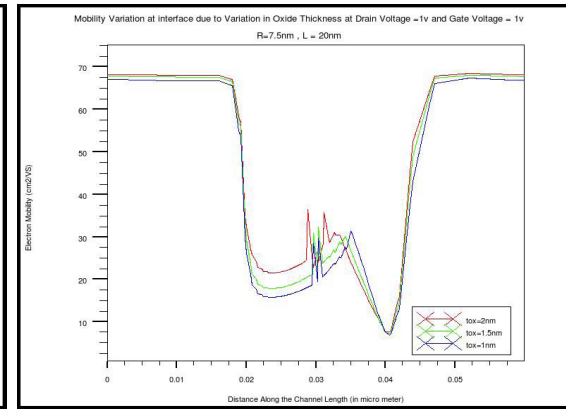

Figure 14: Mobility Variation at interface due to variation in gate oxide thickness of Around at drain voltage = 1v & Gate voltage = 1v.

The figure 13 and figure 14 show that if thickness of oxide (t_{ox}), thickness of silicon tube (t_{si}) and gate length (L) is decreased, mobility is also decreased. It is also found that the effect of t_{ox} on electron mobility is more at interface than centre.

4. CONCLUSION AND FUTURE WORK

To achieve high density, Scaling is done continuously. Due to this scaling, Short Channel Effect (SCE) becomes more dominant factor which does not allow the device for further scaling. So, device fraternity is searching for a replacement of conventional MOSFET. In this regard, a multi-gate device, Surrounding Gate Transistor (SGT), due to its better electrostatic control on channel potential, has gained much interest. The mobility is function of perpendicular electric field and parallel electric field. Perpendicular electric field is a function of gate voltage, gate oxide thickness (t_{ox}), and silicon thickness (t_{si}). Parallel electric field is a function of drain voltage and gate length. Due to quantum mechanical effect, device characteristics are changed such as threshold voltage, drain current, electron density and mobility degradation. It was found that threshold voltage is increased by some milivolt. Due to this drain current is decreased. It is also found that there is a shifting of peak electron density away from Si-SiO_2 interface. Impact of quantum mechanical effect on electron mobility is also found. Due to quantum mechanical effect, effective mobility is decreased. The impacts of device parameter of surrounding gate transistor are also observed. If thickness of oxide (t_{ox}), thickness of silicon tube (t_{si}) and gate length (L) is decreased, mobility is also decreased. It is also found that the effect of t_{ox} on electron mobility is more at interface than centre. The increasing electric field in direction normal to Si-SiO_2 interface as the devices down results in reduction in carrier mobility in MOSFET channel. However, in order to extract the

mobility values, It is necessary to know carrier distribution profile in inversion layer, Since degradation of trans-conductance is also due to the shift of peak electron concentration away from $Si\text{-}SiO_2$ interface due to QM effect, referred to as channel broadening. How to increase the mobility either by using some material or some other things, this can be future work in this area.

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